FPGA forum

FPGA-forum 2026

The 19th FPGA-forum - where the Norwegian FPGA community meets

- FPGA-forum and exhibition: Wednesday 11 and Thursday 12 February 2026
- Workshops: Tuesday 10th

At Royal Garden Hotel (Trondheim)

FPGA-forum er den årlige møteplassen for FPGA-miljøet i Norge. Her samles FPGA-designere, prosjektledere, tekniske ledere, forskere, siste års studenter og de største leverandørene på ett sted for to dagers praktisk fokus på FPGA.

Det blir foredrag fra norske bedrifter om utviklingsmetodikk og praktisk erfaring, universitetene presenterer nye og spennende prosjekter, og leverandørene stiller med aktuelle tekniske innlegg med et minimum av markedsføring. På utstillingen vil du kunne vurdere teknologi, verktøy og tjenester fra de ledende aktørene i bransjen.

FPGA-forum byr i tillegg på en ypperlig anledning til å møtes og utveksle erfaring innenfor FPGA-miljøet i Norge - både i pausene og under det sosiale arrangementet på kvelden.

In English:

FPGA-forum is a yearly event for the Norwegian FPGA community. FPGA-designers, project managers, technical managers, researchers, final year students and the major vendors gather for a two-day focus on FPGA.

There will be presentations from the Norwegian industry about methodology and practical experience, - the universities will present new and exciting projects, and the vendors will have technical presentations with a minimum of marketing. At the exhibition, you can evaluate tools and technology from the leading vendors.

FPGA-forum also provides an excellent opportunity to meet and exchange experience with the Norwegian FPGA-community - during the breaks - and during the official dinner party on Wednesday.

Programme Wednesday, 11 February 2026

(See abstracts and language below)

09.00	Registration and coffee	
Session 1	**Track AB**	
09.15	**Opening** (by Jim Tørresen, UiO and Espen Tallaksen, EmLogic)	
09.30	**Keynote by Eleena Ong, CVP Software Solutions and Applications Engineering at Lattice Semiconductor** **Unlocking the Next Wave of FPGA Innovators with Generative and Agentic AI** (Introduced by: Heidi Skaar Johannessen, Norxe)	
10.30	**Vendor presentations** (3 min. per exhibitor - in alphabetical order) (Chaired by: Espen Tallaksen, EmLogic)	
11:15	**Coffee break (and exhibition)**	
Session 2	**Track A** Session chair: Øyvind Riis, Appear	**Track B** Session chair: Per Gunnar Kjeldsberg, NTNU
11.45	**Accelerating Robotics & Edge AI on Microchip FPGAs** Brian Colgan, Microchip	**Modelling and simulation of FPGA controlled power circuits in standard VHDL** Geir Drange, Inventas
12:15	**Leading Small Form Factor System Devices** Fabian Kluge, Efinix	**Mixed FPGA and Software Simulations with Renode** Even Eide Hansen & Mikkel Mikkelsen, EmLogic
12:45	**Lunch and Exhibition**	
Session 3	**Track A** Session chair: Sigmund Haaland, KD	**Track B** Session chair: Chato Jakobsen, KD
14:00	**Applications of Bitstream Equivalence Checking to High-Assurance FPGA-Based Systems** Jonathan Graf, Graf Research	**High performance DSP processing on AMD AI Engines using new design methodologies** Jan Anders Mathisen, AMD
14:30	**Single-board computer designs based entirely on FPGA and soft-core CPU as replacement for Raspberry Pi and Ultra96 boards** Vladimir Vassilev, Lightside Instruments	
15:00	**GateMate – A European mid-size FPGA with exceptional architecture and reliability** Olaf Jürgens, Cologne Chip	**Effortless Verification: How AI Supercharges Formal Methods with Questa One SFV** Faïçal Chtourou, InnoFour/Siemens EDA
15:30	**Exhibition and Coffee**	
Session 4	**Track A** Session chair: Peter Louis Uller, EmLogic	**Track B** Session chair: Jim Tørresen, UiO
16:00	**Hands-on clock domain crossing** John Aasen, KDA	**Presentation of three nominated Master's projects (for FPGA-forum's award for the best Master's project 2025)**
16:30	**Why the heck can't the FPGA vendors just make their tools usable for real world projects?** Håvard Tørring, Sintef	
17:00	**End of today's presentations**	
19.30	Aperitif in the coffee break area, Royal Garden Hotel	
20.00	Dinner party, Royal Garden Hotel. Including dinner entertainment with Strindens Promenade Orchester	

Programme Thursday, 12 February 2026 (See abstracts and language below)

Session 5	**Track A** Session chair: Heidi Johannesen, Norxe	**Track B** Session chair: Johan Alme, UiB
09.00	**Beyond the Hype: Practical Lessons from Using AI-Tools in FPGA Design** Øyvind Riis, Appear	**From CRA theory to shipping systems** Timo Poikonen, Congatec
09:30	**Tailored FPGA Acceleration for Edge AI: Unlocking Efficiency Beyond GPUs and NPUs** Alex Montgomerie-Corcoran, Heronic	**Data acquisition with RFSoC and data-offloading through RDMA** Hallvard Næss, Zolve
10:00	**Smaller. Cooler. Smarter: Lattice FPGAs' Path to Uncompromised Low Power** Matt Holdsworth, Lattice Semiconductor	**A Bird Flew over a CocoTBs nest** **- A year's experience using CocoTB as the main framework for verification** Sindre Bergsvik Øvstegård, EIDEL
10:30	**Exhibition and Coffee**	
Session 6	**Track A.** Session chair: Per Gunnar Kjeldsberg, NTNU	**Track B** Session chair: Arild Kjerstad, KDA
11:00	**Seeding Trust: Hardware-Based Random Number Generation for Cryptographic Security** Matti Tommiska, Xiphera	**Scoreboards: What, why and how?** Sverre Vigander, Inventas
11:30	**Testing At The Right Time** Tommaso De Vivo, XJTAG	**Assertions in VHDL and UVVM** Espen Tallaksen, EmLogic
12:00	**Lunch and Exhibition**	
Session 7	**Track A** Session chair: Pelle Hovde Eikeberg, EmLogic	**Track B** Session chair: John Aasen, KDA
13:15	**Safe FSM Design for Safety-Critical FPGA Systems: Error Detection and Correction** David Clift, FirstEDA	**Managing and Versioning Gateware Source Code on Git with Hog** Davide Cieri, Max-Planck-Institute for Physics in Munich & Francesco Gonnella, University of Birmingham
13:45	**Building Robots Faster: Modular Hardware/Software Design on SoC FPGAs** Adam Titley, Altera	**FIAT-testing: Testbench analysis using non-invasive fault injection** Yngve Hafting, UiO
14:15	**Coffee break**	
Session 8	**Track AB: Closing Keynotes** Session chair: Arild Kjerstad, Kongsberg	
14:45	**Closing Keynote : Anton Kulyakhtin, Water Linked** When math meets hardware: Optimizing real-time 3D sonar on minimal FPGA resources	
15:30	**Closing Keynote : Sylvain Tertois, EIDEL** **No CPU, No Compromise: Building Reliable FPGA Crypto for Space**	
16:15	Closing words	
16:20	The end	

Keynotes:

- Opening keynote:
  Eleena Ong, CVP Software Solutions and Applications Engineering at Lattice Semiconductor.
  ''Unlocking the Next Wave of FPGA Innovators with Generative and Agentic AI'
  FPGA development has long been the domain of specialized hardware engineers — but the landscape is changing rapidly. Generative AI can now translate high-level requirements into optimized HDL, assist with debug, and surface design insights instantly. Agentic AI takes this further, orchestrating tool flows, running verification loops, and integrating seamlessly with diverse ecosystems. This opens the door not only for hardware and embedded developers, but also for software engineers, AI/ML practitioners, algorithm designers, research scientists, and even domain-specific experts in fields like industrial automation, core and edge computing, automotive, aerospace, and more. In this keynote, we will explore how these rapidly maturing AI technologies can turn FPGA platforms into innovation canvases for a much broader range of developers — lowering adoption barriers, accelerating time-to-market, and sparking new application possibilities.

  Bio:
  Eleena Ong is the CVP Software Solutions and Applications Engineering at Lattice Semiconductor. Eleena joined Lattice with more than 25 years of heritage in the semiconductor industry leading both engineering and marketing organizations, most of that in the FPGA space. Prior to Lattice, Eleena was Vice President of Marketing at Fungible, a startup developing processors for the datacenter market. She also spent many years at Intel / Altera leading the product planning of high and mid-range FPGA portfolio, and planning and deploying board solutions into datacenters and communications applications. Eleena holds a Master of Science degree in Solid State Physics and a Bachelor of Engineering in Electronics and Telecommunications, minoring in Economics. https://www.linkedin.com/in/eleena-ong-58b8367b/.

- Closing keynote Day 2:
  Anton Kulyakhtin, Water Linked
  'When math meets hardware: Optimizing real-time 3D sonar on minimal FPGA resources'
  Water Linked develops compact, yet high-performance underwater navigation systems. At the core of our technology lies a strong synergy between advanced mathematical modeling, signal processing and deep FPGA expertise.

  In this talk, we share insights from developing the Sonar 3D-15 — a real-time 3D imaging sonar built on a surprisingly small Altera FPGA. Achieving real-time 3D point clouds on limited hardware required extreme optimization, creative use of FPGA architecture, and smart algorithmic design.We will also show how modern verification tools like cocotb support efficient testing and optimization.

  The result: a high-performance sonar that demonstrates how mathematical insight and hardware design can combine to achieve what many would consider impossible.

- Closing keynote Day 2:
  Sylvain Tertois, EIDEL
  'No CPU, No Compromise: Building Reliable FPGA Crypto for Space'
  EIDEL is a Norwegian leading designer and supplier of electronics for the defence and aerospace markets. The flexibility and versatility of FPGAs is a major advantage for demanding and low volume products that we deliver. While the current trend on FPGA development is to tightly integrate hardware and embedded software, we have decided for our Nanosatellite Crypto Unit not to use any CPU. This offers advantages when high reliability is required, and modern methodologies for design and especially testing makes the process easier than ever. By focusing on modularity and reuse of functional blocks, we have developed a highly capable and robust system, fully exploiting the parallelism and flexibility inherent to FPGAs.

Prize award for Best FPGA related Master thesis in Norway:

FPGA-Forum's prize is given to the best FPGA-related Master thesis in Norway.

The award committee:

- Dag Andreas Hals Samuelsen, USN
- Heidi Johannessen, Norxe
- Yngve Hafting, UiO

The nominees in alphabetical order:

- **Markus Hjelle Cirotzki**
  'Design of a MOSAIX Emulator Model for ALICE ITS3'
  Supervisors: Johan Alme, Ola Grøttvik (CERN), University of Bergen
- **Even Eide Hansen**
  'Efficient Deep Learning for Real-Time Arrhythmia Detection on Edge FPGAs in Wearable Devices'
  Supervisor: Per Gunnar Kjeldsberg, NTNU
- **Ilya Korneev**
  'Design of the MOSAIX Qualification System for ALICE ITS3'
  Supervisors: Johan Alme, Ola Grøttvik (CERN), University of Bergen

All nominees will present their Master thesis in one of the tracks late on day 1.
The winner will be announced during the dinner party.

List of exhibitors (Wednesday and Thursday):

In alphabetical order:

- Arrow (Altera)
- Avnet Silica (AMD)
- Congatec
- Efinix
- EmLogic
- FirstEDA
- Graf Research
- InnoFour (Siemens EDA)
- Inventas
- Lattice Semiconductor
- Lightside Instruments
- Microchip
- Synective
- Trenz Electronic
- Xiphera
- Adeptor (XJTAG)

Workshops/Tutorials Day 0, Tuesday 10 February:

Workshop 1:

AMD Tech day @FPGA-Forum 2026

AMD and Avnet Silica invites you to a comprehensive presentation of AMD solutions related to FPGAs and Adaptive SoCs. The event will take place 10th February 09:45-16:45 at Royal Garden Hotel in Trondheim – the day before start of FPGA-Forum 2026. The training/presentations will be provided by technical experts from AMD and Avnet Silica. Participation is free of charge and includes lunch and beverages.

Agenda:

1. Update of AMD Adaptive SoC devices portfolio and their applications including embedded x86.
2. Update on AMD development tools, Vivado, Vitis, Vitis HLS and Vitis Model Composer.
3. Design, Develop, Deploy Embedded applications using the new open source “Embedded Development Framework” (EDF)
4. Introduction to MicroBlaze-V and Zephyr.
5. Introduction to current AMD AI/ML Landscape including new Vitis AI.
6. Versal AI Engine architecture and development Flow for DSP applications.

If you would like to attend this event, please register by sending an e-mail with contact details to Jan Anders Mathisen @ Avnet Silica: jananders.mathisen@avnet.eu

Entertainment (during the dinner party):

Strindens Promenade Orchester

Strindens Promenade Orchester is a student orchestra from Studentersamfundet in Trondheim. We primarily play dixie jazz, but we are not afraid of venturing within other musical genres as well. The orchestra consists of 12-15 students. We play for all kinds of local events and businesses, from kindergardens to consulting firms, as well as spontaneous concerts in Nordre gate.

FPGA-forum Program-committee:

- Arild Kjerstad, Kongsberg
- Espen Tallaksen, EmLogic
- Heidi Skaar Johannessen, Norxe
- Jan Anders Mathisen, Silica/Xilinx
- Jim Tørresen, University of Oslo
- Per Gunnar Kjeldsberg, NTNU

Titles and Abstracts for presentations at FPGA-forum 2026

(in company alphabetical order)

Note that written and oral presentations may be in English or Norwegian. Some presenters may also switch to English on Request. Presentations are thus marked 'Written' or 'Oral' and E (English), N (Norwegian) or EoR (English on Request)

Company & Presenter	**Title & Abstract**
Adeptor **Exhibitor**	See XJTAG
Altera Adam Titley **Exhibitor** *Written: E, Oral: E*	**Building Robots Faster: Modular Hardware/Software Design on SoC FPGAs** This presentation explores how modular hardware and software design on SoC FPGAs can significantly accelerate robotics development. By implementing motor control, sensing, and communication as reusable FPGA-based modules, developers gain flexibility, more predictable integration, and faster iteration cycles. The approach supports rapid prototyping, platform reuse, and clean separation of concerns across hardware and software layers. We demonstrate a robot-on-chip workflow and show how this modular methodology improves maintainability, streamlines debugging, and enables scalable robotics designs that can adapt to diverse platforms.
AMD Jan Anders Mathisen **Exhibitor** *Written: E, Oral: EoR*	**High performance DSP processing on AMD AI Engines using new design methodologies** This presentation focuses on the use of AMD Versal AI Engines in implementing high performance DSP functionality. • AI Engine architecture overview • AIE Design methodology and development flows • AI Engine Rapid Prototyping • Independent control of Versal AI Engine partitions • Examples of DSP applications and their performance
Appear Øyvind Riis *Written: E, Oral: E*	**Beyond the Hype: Practical Lessons from Using AI-Tools in FPGA Design** AI for FPGA development is in its infancy but progressing steadily. This presentation shares a real-world evaluation of integrating AI into a professional workflow, focusing on immediate wins like code comprehension, documentation, and onboarding. The session moves beyond the hype to address critical questions: Can AI reliably handle VHDL design and testbench generation? What are its current limits regarding timing analysis? We examine the practical realities of using AI as a force multiplier while navigating the unique constraints of FPGA development.
Arrow **Exhibitor**	See Altera and Microchip
Avnet Silica **Exhibitor**	See AMD
Cologne Chip Olaf Jürgens *Written: E, Oral: E*	**GateMate – A European mid-size FPGA with exceptional architecture and reliability** Manufactured using Globalfoundries advanced 28nm Super Low Power (SLP) process technology, Cologne Chip GateMate FPGAs deliver good performance and energy efficiency. Produced in Germany, they ensure best quality and a robust supply chain at all times. GateMate's architecture is built around an efficient 8-input LUT-tree, enabling complex logic functions with minimal resource usage. Integrated scalable multipliers and 8-input multiplexers provide enhanced arithmetic capabilities and flexible data routing. Cologne Chip's patented in-silicon die-to-die interconnects allow larger FPGAs to be cut from a single wafer and enables considerably more and faster connections between multiple dies in one package. Showing their good performance, quality and reliability already in industrial applications since years, GateMate now also proved it's capabilities for military and space programs thru an extensive radiation test campaign. This presentation will give an overview about Cologne Chip GateMate FPGA technology and give an outlook on next year's release of military and space grade versions.
Congatec Timo Poikonen	**From CRA theory to shipping systems** The EU Cyber Resilience Act turns "security later" into "no CE mark, no market." This makes regulatory compliance to cybersecurity a business-critical factor for Embedded OEMs aiming to

Exhibitor *Written: E, Oral: E*	compete in EU markets. We present a reusable way to most efficiently fulfill the demands of the CRA by leveraging a modular architecture approach that combines standards-based Computer-on-Modules with FPGA-based acceleration, can transform regulatory complexity into manageable, actionable steps. Leveraging application ready hardware and software building blocks makes it possible to: • Cleary allocate security requirements, • Separate responsibilities across teams, and • Efficiently organize compliance across product variants, markets, and lifecycles and finally • Build a verifiable chain of trust for embedded products, paving the way for scalable, sustainable compliance in embedded systems, accelerating Time-to-market, optimizing Non-Recurring Engineering efforts, increasing Return on Investment and lowering Total Cost of Ownership. With this presentation we want to illustrate the available building blocks available next to FPGA's, to create futureproof and CRA compliant designs by OEMs.
Efinix Fabian Kluge **Exhibitor** *Written: E, Oral: E*	**Leading Small Form Factor System Devices** Efinix offers FPGAs in a small form factor that can serve as system controllers, ideally suited for demanding edge applications. The new System in Package (SiP) devices further simplify integration by combining multiple advantages such as lower power consumption, a smaller footprint, and easier PCB integration. Examples include the Ti125 SIP with integrated HyperRAM and the Ti135 SIP with integrated LPDDR4. These devices deliver unprecedented performance in terms of speed and power efficiency. This presentation provides a detailed overview of the new devices and their features, along with exemplary applications.
EIDEL Sylvain Tertois *Written: E, Oral: E*	***** Closing Keynote ***** **No CPU, No Compromise: Building Reliable FPGA Crypto for Space** EIDEL is a Norwegian leading designer and supplier of electronics for the defence and aerospace markets. The flexibility and versatility of FPGAs is a major advantage for demanding and low volume products that we deliver. While the current trend on FPGA development is to tightly integrate hardware and embedded software, we have decided for our Nanosatellite Crypto Unit not to use any CPU. This offers advantages when high reliability is required, and modern methodologies for design and especially testing makes the process easier than ever. By focusing on modularity and reuse of functional blocks, we have developed a highly capable and robust system, fully exploiting the parallelism and flexibility inherent to FPGAs.
EIDEL Sindre Bergsvik Øvstegård *Written: E, Oral: E*	**A Bird Flew over a CocoTBs nest** **- A year's experience using CocoTB as the main framework for verification** In this talk I will share some experiences with using CocoTB as the main verification framework. This talk will not be a introduction or "How to …", (some quick intro for context might be given), but rather a summary of experiences and features which CocoTB offers. I will cover one or maybe two of the topics below, but the idea is to give a "overview" presentation of my own experience using CocoTB professionally. Some topics in no particular order: • Test and build automation by using pytest ‣ Simulation of Altera/Vivado IPs • Ability to develop own and reusable verification objects in python. • Full or partial (flexible) use of pyuvm if one wants to • CocoTB 2.0 (If I get time to use it thorougly) • CocoTB extensions: ‣ cocotbext-axi ‣ cocotbext-spi ‣ cocotbext-i2c • Python integration (transmitting/receiving test-data to and from physical hardware like Oscilloscopes etc) • Some insipiring and motivating examples and projects • What is missing?
EmLogic Even Eide Hansen & Mikkel Mikkelsen **Exhibitor** *Written: E, Oral: E*	**Mixed FPGA and Software Simulations with Renode** This presentation explores a practical approach to verifying FPGA designs that include one or more softcore CPUs by combining RTL simulation with software execution in Renode. Full RTL simulations with software running on softcores are often prohibitively slow, and while techniques such as VVC-based stimulus can help, they do not fully reflect real software behavior. Instead, we use Renode as a functional (non–cycle-accurate) co-simulation environment that runs software much faster while still interacting with the HDL design. We walk through a concrete example: introducing Renode and its co-simulation plugin, configuring buses, GPIOs, and the CPU using configuration files, and implementing a SystemVerilog bridge

	component that connects Renode to the RTL design. We show how to integrate this bridge into an existing design using configurations, and we discuss the startup sequence, including challenges and automation strategies. A live demo showcases a simple design where the real software binary runs in Renode and directly drives and observes the RTL behavior in the simulator. Finally, we share our experiences from adopting this flow, current limitations and rough edges in the Renode ecosystem, some adaptations we made, and why we still see this as a promising direction as the tooling matures.
EmLogic Espen Tallaksen **Exhibitor** *Written: E, Oral: E*	**Assertions in VHDL and UVVM** Assertions can be very useful in detecting problems in your design – and maybe even more important – detecting problems early where the problem arises. Assertions could be used in your design, typically to check assumptions, integration, relations, etc, but also in your testbench, typically to verify specific temporal properties. This presentation will show the use of simple VHDL-based assertions for static and dynamic properties in both design and verification. There will be examples using pure VHDL assertions and the new assertion library in UVVM.
FirstEDA David Clift **Exhibitor** *Written: E, Oral: E*	**Safe FSM Design for Safety-Critical FPGA Systems: Error Detection and Correction** Approximately 17% of FPGA projects experience non-trivial bugs that escape into production. Many of these are logic and functional flaws, including failing FSMs. Have you faced system failures, undetectable faults, and non-compliance with your FSM designs? These issues can compromise reliability, safety, and security. So, how can we ensure FSMs are fit for purpose? This presentation examines practical design methodologies for FSMs in high-reliability and mission-critical environments, considering mitigations for design and operational errors, such as Single Event Upsets (SEUs), which can corrupt state registers and cause system failures in FPGA FSMs. We discuss common design errors and best practices for FSM implementation, including state encoding techniques, protection strategies, and verification approaches. Examples illustrate key principles and trade-offs in resource utilisation and error detection. The presentation provides guidance on selecting appropriate design techniques based on mission requirements and available resources, emphasising practical approaches to avoid typical implementation pitfalls.
Graf Research Jonathan Graf **Exhibitor** *Written: E, Oral: E*	**Applications of Bitstream Equivalence Checking to High-Assurance FPGA-Based Systems** High-assurance systems in aerospace, automotive, nuclear power, and defense increasingly rely on FPGA devices whose deployed behavior is defined solely by the configuration bitstream. Although existing verification flows provide strong evidence at the HDL and physical-netlist levels, they do not validate the bitstream itself, leaving a critical assurance gap. Bitstream Equivalence Checking (BEC) closes this gap by proving logical and physical equivalence between the routed netlist and the configuration bitstream. Enverite® PV-Bit® is a vendor-approved BEC tool that performs this comparison without exposing proprietary bitstream formats or embedded IP to reverse engineering. This work summarizes the application of BEC to four areas central to high-assurance FPGA development: (1) extending verification evidence into the bitstream for regulated safety domains; (2) detecting unintended or malicious bitstream modifications such as hardware Trojans; (3) supporting delta verification for Engineering Change Orders; and (4) validating that vendor modular isolation guarantees are preserved in the deployed bitstream.
Heronic Alex Montgomerie-Corcoran *Written: E, Oral: E*	**Tailored FPGA Acceleration for Edge AI: Unlocking Efficiency Beyond GPUs and NPUs** Edge AI enables access to real-time intelligence within resource-constrained systems. However, at the limits of power, performance and area, Edge AI's demand for low-latency, energy-efficient hardware challenges traditional inference capabilities. The unique requirements of each individual system warrant a tailored approach, extracting the most efficiency out of the underlying silicon. GPUs and NPUs cannot deliver on this due to their generalised, "one-size-fits-all" architecture. Conversely, the fine-grain configurability of FPGAs presents an opportunity to access this efficiency. Despite this opportunity, current solutions do not exploit the benefits of FPGA architectures. Overlay-style designs such as Altera's CoreDLA and AMD's DPU IP deliver on configurability and ease of use, but do not meet the performance requirements of most real-time Edge AI systems. To address this gap in AI performance on FPGAs, Heronic has developed a tool flow for automating the design of bespoke AI accelerator IP for FPGA systems. This approach discovers the most efficient architecture for specific AI applications, utilising close to 100% of the available performance of the target FPGA device. Heronic has demonstrated greater than 50% performance improvement over NVIDIA Jetson Orin NX with Altera FPGAs, and importantly a 28x improvement in TOPS utilisation. This talk will cover how engineers can leverage the benefits of Heronic's approach to accelerator design for Altera devices.

InnoFour/Siemens EDA Faïçal Chtourou, **Exhibitor** *Written: E, Oral: E*	**Effortless Verification: How AI Supercharges Formal Methods with Questa One SFV** The marriage between AI and formal engines marks a significant shift in how static and formal verification are applied to complex hardware designs. Questa One SFV leverages AI to automate assertion generation, optimize solver orchestration, and reduce manual effort in verifying corner-case behaviors. By integrating multiple stimulus-free techniques into a unified flow, it enables broader adoption of formal methods without requiring deep expertise. In this session we will explore how AI-enhanced formal verification improves scalability, efficiency, and accessibility in modern design environments.
Inventas Geir Drange **Exhibitor** *Written: E, Oral: E*	**Modelling and simulation of FPGA controlled power circuits in standard VHDL** FPGAs are commonly used in many applications involving power circuits (motors, voltage converters, signal transmitters, video projectors etc.), but the FPGA testbenches usually lacks a good model of the analog components and loads outside the FPGA, preventing proper closed-loop simulations. A method is presented to model analog circuits in standard VHDL. The method is applied to an example FPGA controlled voltage converter: A VHDL model is established to perform closed-loop simulations with FPGA and converter circuit, the results are compared with a professional circuit simulation tool (spice) and finally with measurements on the actual HW implementation.
Inventas Sverre Vigander **Exhibitor** *Written: E, Oral: E*	**Scoreboards: What, why and how?** What is a scoreboard, and what advantages does a scoreboard methodology bring to your testbench? An introduction to the world of scoreboarding. The talk will go through scoreboarding concepts in the abstract, and does not describe or rely on any specific framework (like UVM, UVVM, CocoTB, etc).
KDA John Aasen *Written: E, Oral: E*	**Hands-on clock domain crossing** This presentation will show some issues we have struggled with when designing correct by design re-usable clock domain crossing mechanisms. It will go into detail with the problems we have seen and how we have solved them.
Lattice Semiconductor Eleena Ong *Written: E, Oral: E*	***** Opening Keynote ***** **Unlocking the Next Wave of FPGA Innovators with Generative and Agentic AI** FPGA development has long been the domain of specialized hardware engineers — but the landscape is changing rapidly. Generative AI can now translate high-level requirements into optimized HDL, assist with debug, and surface design insights instantly. Agentic AI takes this further, orchestrating tool flows, running verification loops, and integrating seamlessly with diverse ecosystems. This opens the door not only for hardware and embedded developers, but also for software engineers, AI/ML practitioners, algorithm designers, research scientists, and even domain-specific experts in fields like industrial automation, core and edge computing, automotive, aerospace, and more. In this keynote, we will explore how these rapidly maturing AI technologies can turn FPGA platforms into innovation canvases for a much broader range of developers — lowering adoption barriers, accelerating time-to-market, and sparking new application possibilities..
Lattice Semiconductor Matt Holdsworth **Exhibitor** *Written: E, Oral: E*	**Smaller. Cooler. Smarter: Lattice FPGAs' Path to Uncompromised Low Power** Tired of compromising performance for power efficiency? In this session, discover the engineering innovations that make Lattice FPGAs the benchmark for ultra-low power consumption. We'll dive into our distinctive approach - combining advancements in silicon processes, architecture, and design methodologies to deliver FPGAs that dramatically lower total cost of ownership. Learn how these technical advantages enable you to create smaller, cooler, and more energy-efficient solutions without compromising the high performance your applications demand.
Lightside Instruments Vladimir Vassilev **Exhibitor** *Written: E, Oral: E*	**Single-board computer designs based entirely on FPGA and soft-core CPU as replacement for Raspberry Pi and Ultra96 boards** The ultimate open-source hardware computer: Running Debian on FPGA with softcore implementation of OpenPOWER CPU (microwatt) and 1Gb Ethernet built with open-source tools. A walk-through of our (Lightside Instruments AS) design and production of a replacement board for proprietary hardware solutions like Raspberry Pi and Ultra96
Microchip Brian Colgan **Exhibitor** *Written: E, Oral: E*	**Accelerating Robotics & Edge AI on Microchip FPGAs** This session explores how Microchip's PolarFire® FPGA and SoC platforms are redefining the boundaries of robotics and artificial intelligence for modern edge applications. Discover how low-power, high-performance FPGAs enable advanced robotics—delivering precise motion control, intelligent vision, and robust security in power- and space-constrained environments. Learn how seamless sensor integration bridges the gap to Nvidia GPUs, unlocking scalable AI acceleration for industrial, automotive, and medical robotics. We'll showcase practical solutions, including real-world customer applications, multi-axis motor control, and embedded vision, while highlighting the

	VectorBlox™ AI engine and the PolarFire Ethernet Sensor Bridge. Join us to see how Microchip and Arrow empower FPGA engineers to build smarter, more efficient, and secure robotic systems for the future.
Siemens EDA **Exhibitor**	See InnoFour
Sintef Håvard Tørring *Written: E, Oral: E*	**Why the heck can't the FPGA vendors just make their tools usable for real world projects?** Problem: Let's face it. When it comes to implementation of real-world projects, the toolchains from the FPGA-vendors prooves to be completely useless. While you can easily click yourself through your first application example while watching someone clicking here and there on a youtube-video, you are doomed to fail once you take a single step out of the virtual playground that the software developers and application engineers operates within. This talk is about opening the fence and taking your first steps into the world of real applications. This is my take on building a solid foundation of tools and processes that enables me to build, debug and maintain complex FPGA projects. This talk is about vivadomake. And to be fair. I named the precedessor to vivadomake alteramake. Requirements/features: • Full control of source files in git • Implementation and simulation of submodules with quick turnaround time • Test and debug and develop submodules in multiple top-levels simultaneously. • Automated connection of submodules to limit tedious and error-prone manual connections • Limit use of block designs to where there's no other way to get things done • Standardized bus interface to ease SW development • Config. of module level debug functions at top-level. Turn ILA-debugging on/off as needed. • Seamless integration between schematics and HDL for readability • Python-based SW development and simultaneous development and debugging of multiple HW targets running on different versions of viviado
The Hog team Davide Cieri, Max-Planck-Institute for Physics in Munich & Francesco Gonnella, University of Birmingham *Written: E, Oral: E*	**Managing and Versioning Gateware Source Code on Git with Hog** Coordinating firmware development among many international collaborators is becoming a widespread challenge. Hog (HDL-on-git) is a powerful set of Tcl/Shell scripts designed to facilitate the management of HDL code for FPGAs with Git. It guarantees synthesis and Place and Route (P&R) reproducibility and assures the traceability of output binary files. Key Features: 1. Reproducibility: Full control over source and configuration files, ensuring consistent synthesis and P&R results. 2. Traceability: Each binary firmware file embeds the git tag and commit SHA, allowing retrieval of the corresponding source code from the repository at any time. 3. Continuous Integration (CI): Templates for setting up a CI workflow to build and simulate HDL projects using GitLab CI/CD or GitHub Actions. 4. Compatibility: Works seamlessly with major HDL IDEs like AMD Vivado, ISE, Altera Quartus, and MicroSemi Libero.
UiO Yngve Hafting *Written: E, Oral: EoR*	**FIAT-testing: Testbench analysis using non-invasive fault injection** Verification is an integral part of hardware development. Detection and correction of implementation defects in an early stage of development is known to reduce development time and cost. Errors in the verification testbench can lead to a reported false higher functional coverage metric and undiscovered defects in the implementation. We introduce an integrated methodology to validate the testbench prior to functional verification of the implementation. To validate testbench correctness, module output or state is altered by using non-invasive fault injection. Applied right, this methodology come at a low cost in terms of human effort and computation. Examples of how this is implemented are given in both VHDL and Python for both RTL and TLM based testbenches. Demo video and examples can be found at: https://github.com/yngveha/FIAT
Xiphera Matti Tommiska **Exhibitor** *Written: E, Oral: E*	**Seeding Trust: Hardware-Based Random Number Generation for Cryptographic Security** The quality and security of random number generation are foundational to modern cryptographic applications. In this presentation, Xiphera's CEO Matti Tommiska explores the design, implementation, and deployment of True Random Number Generators (TRNGs) and Pseudorandom Number Generators (PRNGs) on FPGAs. The presentation covers hardware-based entropy sources, post-processing techniques, and statistical validation methods to ensure cryptographic robustness. It also demonstrates how a hybrid architecture – the combination of a TRNG including an internal entropy source with a high-throughput PRNG – can be efficiently integrated into FPGA logic to deliver scalable and cryptographically secure randomness. Real-world performance benchmarks, design trade-offs, and security implications are discussed, offering insights into deploying FPGA-based random number generation in real-world systems and applications.

XJTAG Tommaso De Vivo **Exhibitor** *Written: E, Oral: E*	**Testing At The Right Time** We've all seen the cost that testing at the wrong time can cause. Whether you're familiar with the 1-10-100 rule, shift-left mindsets or design-for-test principles, what you really need is not just theories but concrete steps you can take to minimise the cost of quality both in development and production. The talk will cover the pros and cons of specific testing approaches and help you make the right choice for your next project.
Zolve Hallvard Næss *Written: E, Oral: E*	**Data acquisition with RFSoC and data-offloading through RDMA** RFSoC FPGAs can gather and process huge volumes of data, making them ideal for highbandwidth acquisition. But how do you offload all that data efficiently? The UltraScale+ platform offers a 100G Ethernet interface, which seems like the perfect solution - until you face the challenge of handling a relentless 100 Gbps stream at the receiving end. That's where Remote Direct Memory Access (RDMA) comes to the rescue. By streaming data directly into receiver memory, RDMA bypasses the CPU, minimizing copy overhead and freeing it for higherlevel tasks. This presentation describes how this approach was used at Alcatel Submarine Networks (ASN) in an optical Distributed Acoustic Sensing product, enabling efficient realtime acquisition, transfer and storage of sensor data streams.
Water Linked Anton Kulyakhtin *Written: E, Oral: E*	***** Closing Keynote ***** **When math meets hardware: Optimizing real-time 3D sonar on minimal FPGA resources** Water Linked develops compact, yet high-performance underwater navigation systems. At the core of our technology lies a strong synergy between advanced mathematical modeling, signal processing and deep FPGA expertise. In this talk, we share insights from developing the Sonar 3D-15 — a real-time 3D imaging sonar built on a surprisingly small Altera FPGA. Achieving real-time 3D point clouds on limited hardware required extreme optimization, creative use of FPGA architecture, and smart algorithmic design.We will also show how modern verification tools like cocotb support efficient testing and optimization. The result: a high-performance sonar that demonstrates how mathematical insight and hardware design can combine to achieve what many would consider impossible.