FPGA forum

Full PROGRAMME per 17 January

Please note minor changes in the programme should be expected.

FPGA-forum 2025

The 18th FPGA-forum – where the Norwegian FPGA community meets

- FPGA-forum and exhibition: Wednesday 5th and Thursday 6th February 2025
- Workshops: Tuesday 4th

At Royal Garden Hotel (Trondheim)

FPGA-forum er den årlige møteplassen for FPGA-miljøet i Norge. Her samles FPGA-designere, prosjektledere, tekniske ledere, forskere, siste års studenter og de største leverandørene på ett sted for 2 dagers praktisk fokus på FPGA.

Det blir foredrag fra norske bedrifter om utviklingsmetodikk og praktisk erfaring, universitetene presenterer nye og spennende prosjekter, og leverandørene stiller med aktuelle tekniske innlegg med et minimum av markedsføring. På utstillingen vil du kunne vurdere teknologi, verktøy og tjenester fra de ledende aktørene i bransjen.

FPGA-forum byr i tillegg på en ypperlig anledning til å møtes og utveksle erfaring innenfor FPGA-miljøet i Norge - både i pausene og under det sosiale arrangementet på kvelden.

In English:

FPGA-forum is a yearly event for the Norwegian FPGA community. FPGA-designers, project managers, technical managers, researchers, final year students and the major vendors gather for a two-day focus on FPGA.

There will be presentations from the Norwegian industry about methodology and practical experience, - the universities will present new and exciting projects, and the vendors will have technical presentations with a minimum of marketing. At the exhibition, you can evaluate tools and technology from the leading vendors.

FPGA-forum also provides an excellent opportunity to meet and exchange experience with the Norwegian FPGA-community – during the breaks – and during the official dinner party on Wednesday.

Programme Wednesday, 5 February, 2025 (See abstracts below)

(Flags show spoken language. means English on request. Slide language is normally the same as the title. If in doubt check appendix.)

09.00	Registration and coffee	
Session 1	**Track AB**	
09.15	**Opening** (by Jim Tørresen, UiO and Espen Tallaksen, EmLogic)	
09.30	**Keynote by Anthony Cartolano,** **FPGAAIPQCCRABBQ, or How to Decode (Survive?) The Cyber Storm** (Introduced by: TBD)	
10.30	**Vendor presentations** (3 min. per exhibitor - in alphabetical order) (Chaired by: Espen Tallaksen, EmLogic)	
11:15	**Coffee break (and exhibition)**	
Session 2	**Track A** Session chair	**Track B** Session chair:
11.45	**Leveraging Pytest for HIL-testing: A quick start guide** Peter Uran, Zolve	**Targeting the highest safety standards in single chip solutions** Jan Anders Mathisen & Tryggve Mathiesen, Avnet Silica
12:15	**Introduction to Accelerated PCBA Testing and Programming** Tommaso De Vivo, XJTAG	**Simplified and Efficient Data Flow with AXI-Stream** Rune Bæverrud, EmLogic
12:45	**Lunch and Exhibition**	
Session 3	**Track A** Session chair:	**Track B** Session chair:
14:00	**Simple and Efficient FPGA Verification with UVVM and HDLRegression** Marius Elvegård, Inventas	**Lattice introduces Nexus 2 - the low-power FPGA with Advanced Connectivity and PQC Security** Matt Holdsworth, Lattice
14:30	**Experiences from teaching digital system design using Python-based testbenches** Yngve Hafting, UiO	**Mainstream low power, high speed FPGAs for edge application** NN, Efinix
15:00	**Dynamic High-Level Synthesis with R-HLS** Magnus Själander, NTNU, IDI	**Example Designs to kickstart your Agilex 5 projects** Mark Frost, Altera
15:30	**Exhibition and Coffee**	
Session 4	**Track A** Session chair:	**Track B** Session chair:
16:00	**Living with a build system** Jørgen Linnerud, Cisco	**Presentasjon av Masteroppgaver** **(For FPGA-forums pris for beste Masteroppgave 2024)**
16:30	**Efficient Verification for Robust Products** Loan Guilbaud, Appear	
17:00	**End of today's presentations**	
19.30	Aperitif TBD, Royal Garden Hotel	
20.00	Dinner party, Royal Garden Hotel. Including dinner entertainment with Candiss	

Programme Thursday, 6 February, 2025 (See abstracts below)

(Flags show spoken language. means English on request. Slide language is normally the same as the title. If in doubt check appendix.)

Session 5	**Track A** Session chair:	**Track B** Session chair:
09.00	**Optimising FPGA Development: From Design to Verification with Practical Methodologies** David Clift, FirstEDA	**FPGA Vision: Building Scalable AI-Infused Camera Solutions** Alexey Lopich, Altera
09:30	**FFI's Multifunction RF demonstrator based on 3rd generation AMD RFSoC** Idar Norheim-Næss, FFI	**Breaking Boundaries: AI-Driven Verification Innovation** Faïçal Chtourou, Siemens EDA
10:00	**FPGA-Based Post-Quantum Secure Boot for Critical Computing Platforms** Matti Tommiska, Xiphera	**Good enough and AI in time delivery for cost optimized Embedded FPGA systems** Tryggve Mathiesen, AMD
10:30	**Exhibition and Coffee**	
Session 6	**Track A.** Session chair:	**Track B** Session chair
11:00	**Standardized Computer-on-Modules optimize customized FPGA application designs** Timo Poikonen, congatec	**Co-simulation in a UVVM-based testbench** Simon Voigt Nesbø, Inventas
11:30	**Powering FPGAs – A programmable power supply that is truly one size fits all** Olaf Jürgens, DIMAC Red	**Modern VHDL Testbenches; An AXI-Stream example – first using BFMs, then VVCs** Espen Tallaksen, EmLogic
12:00	**Lunch and Exhibition**	
Session 7	**Track A** Session chair:	**Track B** Session chair:
13:15	**PLPS Interface Generator (PPG)** Geir Åge Noven, KDA	**Lattice solves USB3 video integration challenges with industry's first USB3 enabled FPGA** Matt Holdsworth, Lattice
13:45	**FPGAs in the development of the MOSAIX test system** Ilya Korneev, and Markus Hjelle Cirotzki, UiB	**Reuse of complex target tests in pre-silicon validation and the advantages of model defined and synthesizable generator and analyzer cores.** Vladimir Vassilev, Lightside Instruments
14:15	**Coffee break**	
Session 8	**Track AB: Closing Keynotes** Session chair:	
14:45	**Closing Keynote: Erik Swensen, Medistim** Succeeding in the global medical device market: How FPGA-technology can accelerate time to market and support effective life cycle management	
15:30	**Closing Keynote: Knut Krogstad, 3D Perception** The future of FPGA code development'	
16:15	Closing words	
16:20	The end	

Workshops/Tutorials Day 0, Tuesday 4 February:

FPGA-forum workshops are handled 100% by each workshop organiser.

Workshop 1: Security in FPGA based systems…

Time: 4 February: 11:00-16:30

Security is becoming a ever-more important topic, but what does it mean to the FPGA designer? Attend this workshop to find out more about foundational security topics like authentication and encryption and how to use them to protect your IP (live demos!) In addition we will cover more advanced topics like keys, key management through to platform attestation. The focus will be on how the Agilex 5 secure device manager enables these security features.

By Tony Cartolano, Altera

Registration and more info: https://forms.office.com/r/6qvw37F6BH

Workshop 2: Build your RISC-V system on a Low Power FPGA

Time: 4 February: 12:30-16:45

Learn how to build and program your RISC-V processor system with Lattice Radiant and Propel Tools on free Certux-NX Low Power CRUVI board. When all up and running you can take the board with you and continue you company design at work

By Matt Holdsworth and René Kappel Jensen

Registration and more info: https://forms.office.com/r/PNJmnGVLzw

Keynotes:

- Opening keynote:
  Anthony Cartolano, Altera FPGA Security Expert.
  'FPGAAIPQCCRABBQ, or How to Decode (Survive?) The Cyber Storm'
  Cybersecurity has captured headlines with an alarming increase in frequency. Between AI, quantum computers, software platforms, and government inquiries, it has been difficult to avoid daily disruptions, much less complete a reasonable product development cycle. In this talk, we'll examine how recent trends, including artificial intelligence, post-quantum cryptography and more are placing incredible demands on product designers. We'll show how and why FPGAs are uniquely suited to help designers both survive the current storm of rapidly changing requirements and prepare to respond to challenges throughout their lifecycle. Finally, we'll discuss how FPGAs are already prepared to meet the requirements of the Cyber Resilience Act.

  Bio:
  Tony Cartolano is a senior engineer at Altera and currently leads the Security Factory Applications team.
  He holds an M.S in Electrical and Computer Engineering from Carnegie Mellon University. He designed various aspects of IBM z/Series Millicode from 2010-2016, including high performance interrupt and transactional memory routines. He joined Altera in 2016 as a Regional Applications engineer focused on Nios and ARM subsystems before moving to the Factory Applications team in 2019. Tony is an influential voice of the customer and is dedicated to building innovative and easy to use security solutions in service of Altera's goal to be the worldwide leading FPGA company.

- Closing keynote Day 2:
  Erik Swensen, Medistim
  'Succeeding in the global medical device market: How FPGA-technology can accelerate time to market and support effective life cycle management'
  Medistim delivers ultrasound-based technology for quality control of cardiovascular surgical procedures to the global market. To be competitive in the volume segment we operate, we need technology that is cost effective for low to mid volumes, short time-to-market with product updates, possibilities for post-deployment updates and support for long and stable component availability. Modern FPGA technology has shown to offer all of this , and with close collaboration with Norwegian companies like Aurotech Ultrasound, we have been able to put attractive products on the global market and deliver a continuous growth for the last 20 years

- Closing keynote Day 2:
  Knut Krogstad, 3D Perception
  'The future of FPGA code development'
  FPGA technologies have enabled anyone to create products that previously required huge investments in ASICs. Developers need to cover multiple disciplines and handle increasing complexity, and the learning curve can be steep. We will discuss competence needs, methodologies, tools and other topics to generate code that is maintainable, portable, fast, and with high quality. The author has followed the technology since the early days, and has developed FPGA based solutions for more than 30 years.

Price award for Best FPGA related Master thesis in Norway:

FPGA-Forum's price is given to the best FPGA related Master thesis in Norway.

The award committee:

- Dag Andreas Hals Samuelsen, University College of Southeast Norway (USN)
- Heidi Skaar Johannessen, Norxe
- Johan Alme, University of Bergen

The nominees in alphabetical order:

- **Sigmund Haaland:**
  "*Investigating the Viability of FPGAs as General Purpose Accelerators"*
  Supervisors: Kristoffer Robin Stokke (Huddly and UiO), Jim Tørresen (UiO) and Håkon Kvale Stensland (Simula and UiO)
  Department of Informatics, University of Oslo (UiO)
- **Daniel Vorhaug:**
  "Hyperspectral Image Compression Accelerator On FPGA Using CCSDS 123.0-B-2"
  Supervisors: Milica Orlandic and Samuel Boyle
  Department of Electronic Systems, NTNU

All nominees will present their Master thesis in one of the tracks late on day 1.
The winner will be announced during the dinner party.

List of exhibitors (for Wednesday and Thursday):

In alphabetical order:

- Arrow (Altera)
- Avnet Silica (AMD)
- Congatec
- Efinix
- Eidel
- EmLogic
- FirstEDA (Aldec)
- Innofour (Siemens EDA)
- Inventas
- Lattice
- Lightside Instruments
- Microchip
- Synective
- Trenz Electronic
- Xiphera
- XJTAG (Adeptor)

Entertainment (during the dinner party):

The “Pink Student choir” in Trondheim: Candiss

Candiss is a female student choir from Studentersamfundet in Trondheim. We are students from all different campuses at NTNU with one thing in common, that we love to sing and joke around! We are easy to recognize with our pink overalls, and we have been a part of the life in the city since 1982.

Foto: foto.samfundet.no

FPGA-forum Program-committee:

- Arild Kjerstad, Kongsberg
- Heidi Skaar Johannessen, Norxe
- Jan Anders Mathisen, Silica/Xilinx
- Jim Tørresen, University of Oslo
- Per Gunnar Kjeldsberg, NTNU
- Espen Tallaksen, EmLogic

Titles and Abstracts for presentations at FPGA-forum 2025

(In company alphabetical order)

Note that written and oral presentations may be in English or Norwegian. Some presenters may also switch to English on Request
Presentations are thus marked 'Written' or 'Oral' and E (English), N (Norwegian) or EoR (English on Request)

Company & Presenter	**Title & Abstract**
3D perception Knut Krogstad *Written: E, Oral: E*	***** Closing Keynote ***** **The future of FPGA code development** FPGA technologies have enabled anyone to create products that previously required huge investments in ASICs. Developers need to cover multiple disciplines and handle increasing complexity, and the learning curve can be steep. We will discuss competence needs, methodologies, tools and other topics to generate code that is maintainable, portable, fast, and with high quality. The author has followed the technology since the early days, and has developed FPGA based solutions for more than 30 years.
Adeptor **Exhibitor**	See XJTAG
Altera Anthony Cartolano *Written: E, Oral: E*	***** Opening Keynote ***** **FPGAAIPQCCRABBQ, or How to Decode (Survive?) The Cyber Storm** Cybersecurity has captured headlines with an alarming increase in frequency. Between AI, quantum computers, software platforms, and government inquiries, it has been difficult to avoid daily disruptions, much less complete a reasonable product development cycle. In this talk, we'll examine how recent trends, including artificial intelligence, post-quantum cryptography and more are placing incredible demands on product designers. We'll show how and why FPGAs are uniquely suited to help designers both survive the current storm of rapidly changing requirements and prepare to respond to challenges throughout their lifecycle. Finally, we'll discuss how FPGAs are already prepared to meet the requirements of the Cyber Resilience Act.

AMD Tryggve Mathiesen *Written: E, Oral: E*	**Good enough and AI in time delivery for cost optimized Embedded FPGA systems** In the context of AI inference, we face challenges embedded performance scalability requirements, high demands of compute and storage. These challenges are even more constrained in FPGA embedded systems, with constantly evolving range of applications and algorithms for self-contained system or edge sensors. The FPGA specific trade-offs are constrained by Performance, Latency, Area, and Power as well as suitable AI Inference tool flow. In this talk, we explore how embedded FPGA devices and adaptive solutions can delivering post-production hardware specialization and SW co-designed algorithms. With a quotative approach, using constraining metrics, we will compare CPU, GPU, AI HW Accelerator, NPU(DPU), Vector extensions, embedded FINN inference methods – also rate the AI inference with respect to FPGA Embedded suitability. This will result in embedded optimized FPGA AI systems which provide performance scalability, FPGA reduction in size and power footprint – preserving full flexibility for embedded FPGA applications while maintaining scalability, tuneability and standardized AI Inference flow.
Appear Loan Guilbaud *Written: E, Oral: E*	**Efficient Verification for Robust Products** Developing FPGA-based products requires rigorous and exhaustive testing to guarantee reliability and robustness when put in operation. Verification is especially critical when modifying a module used across multiple projects: how are you certain you did not break anything? In this presentation, we will explore how we leverage Gitlab, a DevOps platform, to maintain and increase the general quality of our VHDL codebase and thus our FPGA projects. We will dig into our verification processes, including testbenches, timing analysis, formal verification, linting and more, and demonstrate how we can successfully manage over 50 products and 80 libraries with a team of 12 FPGA engineers, without impacting the product timelines.
Arrow (Altera) Mark Frost, Altera **Exhibitor** *Written: E, Oral: E*	**Example Designs to kickstart your Agilex 5 projects** An overview of the many Example Designs available for our new mid-range FPGA family. Covering simplistic use of IPs through to full solutions from Video, Industrial and Communication sectors. Includes some live demos too!
Arrow (Altera) Alexey Lopich, Altera **Exhibitor** *Written: E, Oral: E*	**FPGA Vision: Building Scalable AI-Infused Camera Solutions** Most modern cameras are underpinned by some form of intelligence, from a rudimentary tuning of image signal processor (ISP) parameters for constrained setup to automatic control of exposure, color balance, and focus (3A) for changing environments. Traditionally, such mechanisms are based on computer vision-based algorithms that analyze the scene based on abstracted numerical indicators (histograms, statistics, etc.). Recent advances in ML accelerators enabled on-the-fly content analysis. Such processing has conventionally been performed on fully processed RGB images and used to perform various object detection and recognition functions for security, video conferencing, automotive, and other end-user applications. However, enabled by FPGAs close NPU+ISP integration, flexibility in "tapping" points, and network-optimized architectures unlocked natural synergy between image processing and AI. In this talk we discuss how to build a smart camera solution with a native AI inference engine and flexible imaging pipeline integration. We examine the use of in-depth content analysis and salient feature extraction to fine-tune existing ISP parameters for target human or machine vision applications. Additionally, we will review the methodology to design such systems with inherent portability built-in to facilitate porting solutions across various devices and development kits with ease.

Avnet Silica / AMD Jan Anders Mathisen, Tryggve Mathiesen **Exhibitor** *Written: E, Oral: TBD*	**Targeting the highest safety standards in single chip solutions** A practical approach to how new architectural features, IP, tools and methodologies allows the highest safety standards to be addressed with single chip SoC/FPGAs solutions in industrial, medical and automotive applications.
Cisco Jørgen Linnerud *Written: E, Oral: ?*	**Living with a build system** For the past two decades, Cisco at Lysaker has been utilizing FPGAs in collaboration video devices. Throughout this period, various tools and build system features have been developed to facilitate FPGA integration into new projects while maintaining high-quality for existing products within a CI/CD environment. This talk will address some of the methods and the strategies Cisco at Lysaker has adopted and the challenges encountered as the world continues to evolve.
congatec Timo Poikonen **Exhibitor** *Written: E, Oral: E*	**Standardized Computer-on-Modules optimize customized FPGA application designs** Combining customized FPGA designs with standardized Computer-on-Modules (COMs) delivers a high-performance solution with minimal design effort, fast time-to-market, exceptional scalability, and long-term upgradeability—ultimately improving TCO, ROI, and sustainability. By using standardized COMs such as SMARC, COM-HPC, or COM Express, most of the design-in work for x86 or Arm CPUs is already done by the module vendor. These application-ready super-components allow designers to focus entirely on application-specific needs via a customizable carrier board that holds the FPGA, onto which the COM is plugged. This approach enhances design reliability, reduces costs, and accelerates time-to-market. At the same time, COMs offer high scalability across multiple x86 and Arm performance classes, optimizing size, weight, cost, and power. With standardized interfaces and dimensions, COMs are easily interchangeable within the same standard, enabling seamless application upgrades even years post-deployment. As such, COMs are the ideal partner for any custom FPGA application design.
DIMAC Red Olaf Jürgens *Written: E, Oral: E*	**Powering FPGAs – A programmable power supply that is truly one size fits all** In Edge AI applications as in all modern systems, powering FPGAs is becoming increasingly more complex with multiple power domains each with specific and often disparate requirements. Voltage programmability, rails sequencing, dynamic voltage scaling, are all aspects that need to be dealt with when developing a suitable power train. This accumulation of sometimes contradicting requirements leads to undesired tradeoffs in terms of performance, size and efficiency. A single-device fully programmable power solution tailored specifically to power FPGAs delivers substantial benefits, including enhanced power density, simplified design, and streamlined integration, ultimately reducing PCB footprint and thermal challenges. This solution not only addresses the dynamic power needs of advanced FPGAs but also ensures enough flexibility to adapt and scale to different families of devices. The result is an optimized power architecture that accelerates time-to-market, reduces design complexity, and improves reliability—making it an ideal choice for next-generation FPGA-driven systems. This presentation will showcase the innovative Integrated Voltage Regulator (IVR) from Empower Semiconductor as a simple, flexible yet performing solution to power most modern FPGAs.
Efinix NN *Written: E, Oral: E*	**Mainstream low power, high speed FPGAs for edge application** In this session we will show our 3 different FPGA Families which can be used at different application. All together have the disruptive XLR architecture which gives us low power and high speed at the same time at a very small Die size. These items are very important for edge applications as power and size matters. To support as well high-speed interfaces, we will give you a quick overview about the supported interfaces like PCI-E (up to Gen4), 10GE and more. In addition, we will introduce our available evaluation systems our AI solution together with our free of charge Software to quickly get up to speed for your project.

EmLogic Rune Bæverrud **Exhibitor** *Written: E, Oral: N*	**Simplified and Efficient Data Flow with AXI-Stream** Clean and simple IP interfaces are crucial for efficient development. A common understanding of these reduces the number of errors and allows developers to focus on functionality instead of interfaces. This also minimizes the need for documentation. A common understanding also simplifies the methodology, and there are examples of how good methodology in module descriptions can more than halve development time. As an example, I will show how we can streamline packet processing for maximum performance.
EmLogic Espen Tallaksen **Exhibitor** *Written: E, Oral: E*	**Modern VHDL Testbenches; An AXI-Stream example – first using BFMs, then VVCs** Do you want to see how easily you can verify your FPGA? Join in to see this exemplified with a testbench for an AXI-stream based data flow design – using UVVM, which is currently used by more than one third of all European FPGA designers. Most testbenches verifying a complex DUT are relatively unstructured and difficult to understand, modify, extend, maintain and reuse. You can often easily reduce the verification time by at least a factor of two by having a well structured and easy-to-understand test harness, - and writing commands at a higher abstraction level – allowing a good and complete test case overview by just looking at a simple test sequencer with easy-to-understand high-level commands. This presentation will first show how interface handling procedures (BFMs) can be applied in a very simple way to verify a DUT. Then we will show how a more advanced testbench using verification components, models, scoreboards and high-level transactions will allow more thorough verification of more complex DUT scenarios in a very structured and simple way.
FFI Idar Norheim-Næss *Written: E, Oral: EoR*	**FFI's Multifunction RF demonstrator based on 3rd generation AMD RFSoC** At FFI we have in development a multifunction RF demonstrator, designed as a common platform for experimenting with the possibilities and limitations of simultaneous measurements of passive and active RF sensing. The demonstrator started out using an AMD ZCU111 evaluation board in S-band (3.2 GHz) with two reception channels for direction finding, but has now evolved into a 16 channel digital active phased array system in C-band (5.6 GHz) with the AMD ZCU216 board at the center. Still in active development, the current status will be presented with focus on the hardware and some discussion on the possibilities (and limitations) of using the RFSoCs.
FirstEDA David Clift **Exhibitor** *Written: E, Oral: E*	**Optimising FPGA Development: From Design to Verification with Practical Methodologies** This presentation introduces key methodologies and tools essential to FPGA design and verification, focusing on optimising development processes to ensure functional correctness and performance. We will explore top-down and bottom-up design strategies and compare open-source and commercial tools for FPGA design. The role of continuous integration (CI) will also be highlighted, emphasising its value in automating testing and accelerating development cycles.
InnoFour **Exhibitor**	See Siemens EDA
Inventas Marius Elvegård **Exhibitor** *Written: E, Oral: EoR*	**Simple and Efficient FPGA Verification with UVVM and HDLRegression** UVVM and HDLRegression are powerful tools for verifying and simulating VHDL testbenches. UVVM is designed to be user-friendly and easy to understand, while allowing efficient and structured testbenches and test environments. HDLRegression simplifies the simulation process by offering easy setups and configurations, so you can focus on writing quality testbenches instead of dealing with complex simulation tools, tcl files and compile order. In this presentation, I will show how quickly and easily a UVVM simulation environment can be set up and prepared for simulation with HDLRegression. I will demonstrate that advanced FPGA verification does not have to be complicated, and how UVVM and HDLRegression can simplify and improve the verification process.

Inventas Simon Voigt Nesbø **Exhibitor** *Written: E, Oral: EoR*	**Co-simulation in a UVVM-based testbench** Verification of RTL code is a critical step in FPGA design. Most developers prefer using native design languages like VHDL or SystemVerilog for verification, along with popular frameworks like UVVM. However, the RTL design is seldom used in isolation; in most cases, there are several communication interfaces, drivers, or support software it must interact with, which may even run on an embedded CPU core within the FPGA. Integration and system testing of software with the FPGA design often end up being done ad-hoc and sporadically against the running hardware. Co-simulation, which is the ability to interact with a running HDL simulation from a foreign language or process, is necessary to bridge an RTL simulation with support software. It enables more advanced use cases, such as regression testing within a continuous integration pipeline. This presentation will demonstrate how to adapt an existing UVVM testbench for co-simulation using foreign language interfaces like VPI or VHPI/VHPIDIRECT.
KDA Geir Åge Noven *Written: E, Oral: E*	**PLPS Interface Generator (PPG)** Abstract: The PLPS Interface Generator is a KDA defined way of defining the interface between PL (Programmable Logic) and PS (Processing System) in an AMD SoC (System on Chip). The design goal was to encapsulate low level features of both the PL and PS domain into modules with autogenerated code and library modules/functions.
Lattice Semiconductor Matt Holdsworth **Exhibitor** *Written: E, Oral: E*	**Lattice solves USB3 video integration challenges with industry's first USB3 enabled FPGA** A typical challenge for video integration is the limited number of video interfaces offered by the CPU. Lattice addresses this connectivity challenge with CrossLinkU-NX, the industry's first USB3 enabled FPGA. With integrated USB 3.2 Gen 1 (5 Gbps) Controller/PHY and ultra-low power FPGA architecture, Lattice is enabling a new class of USB3 vision applications in areas such as Edge AI and Always-On Video.
Lattice Semiconductor Matt Holdsworth **Exhibitor** *Written: E, Oral: E*	**Lattice introduces Nexus 2 - the low-power FPGA with Advanced Connectivity and PQC Security** System design has never been more challenging. Coupled with the typical demands to reduce power and improve performance, next generation architectures will be subject to new requirements around Security, AI and even form-factor. Lattice addresses all of these challenges with Nexus 2 - the perfect device for low-power, small form-factor designs that cannot compromise on performance or security
Lightside Instruments Vladimir Vassilev **Exhibitor** *Written: E, Oral: E*	**Reuse of complex target tests in pre-silicon validation and the advantages of model defined and synthesizable generator and analyzer cores.** In this presentation we (Lightside Instruments AS) will demonstrate our approach of using high level management model specifications (YANG RFC7950) and transactional protocol (NETCONF 6241) to orchestrate the behavior of generators and analyzers used in pre-silicon validation. We will use as example test a python implementation of the RFC2544 (Benchmarking Methodology for Network Interconnect Devices) specified target test that can be executed with any device with network interfaces that implements the model. We will use the cocotb simulation environment with iverilog simulator and a minimal socket communication handler controlling the progress of the simulation, reading and writing AXI registers, and handling interrupt events. We will use our open-source 1Gb Ethernet GMII traffic generator and analyzer cores implementing the draft-ietf-bmwg-network-tester-cfg-05 model. We will run the same test against the simulated environment and a FPGA based embedded system implementation.

Medistim Erik Swensen *Written: E, Oral: E*	***** Closing Keynote ***** **Succeeding in the global medical device market: How FPGA-technology can accelerate time to market and support effective life cycle management** Medistim delivers ultrasound-based technology for quality control of cardiovascular surgical procedures to the global market. To be competitive in the volume segment we operate, we need technology that is cost effective for low to mid volumes, short time-to-market with product updates, possibilities for post-deployment updates and support for long and stable component availability. Modern FPGA technology has shown to offer all of this , and with close collaboration with Norwegian companies like Aurotech Ultrasound, we have been able to put attractive products on the global market and deliver a continuous growth for the last 20 years
NTNU, IDI Magnus Själander *Written: E, Oral: E*	**Dynamic High-Level Synthesis with R-HLS** Dynamically scheduled hardware enables high-level synthesis (HLS) for applications with irregular control flow and latencies, which perform poorly with conventional statically scheduled approaches. Since dynamically scheduled hardware is inherently data flow based, it is beneficial to have an intermediate representation (IR) that captures the global data flow to enable easier transformations. R-HLS is an intermediate representation developed at the Computer Architecture Lab, NTNU, which is specifically targeted for efficient optimization of dynamically scheduled hardware. R-HLS explicitly models control flow decisions, routing, and memory. Expressing the control flow as part of the data flow reduces the need for complex optimizations to extract performance and enables easy conversion to parallel circuits. Our results show that R-HLS exposes parallelism, resulting in fewer executed cycles and a 10% speedup on average, compared to the state-of-the-art in dynamic HLS. These results are achieved with a significant reduction in resource utilization, such as a 79% reduction in lookup-tables and 22% reduction in flip-flops, on average.
Siemens EDA Faïçal Chtourou, **Exhibitor** *Written: E, Oral: E*	**Breaking Boundaries: AI-Driven Verification Innovation** AI is a buzzword these days, but what does it truly mean for our industry? In this presentation, we'll delve into the opportunities and challenges brought by AI and how they can spur innovation and growth. At Siemens, we've been leveraging AI even before the current hype, continuously integrating these technologies into our tools. You'll discover not only how we've successfully implemented AI so far, but also what exciting developments you can anticipate in the near future.

UiB Ilya Korneev, and Markus Hjelle Cirotzki *Written: E, Oral: ?*	**FPGAs in the development of the MOSAIX test system** The ALICE experiment at CERN studies quark-gluon plasma made in the collisions between heavy ions. The detector closest to the interaction point is a vertex detector called the Inner Tracking System (ITS). This detector is made up of chips called ALPIDE, which consists of monolithic active pixel sensors (MAPS). These chips are arranged in rigid staves in seven layers around the beam pipe. Beginning in 2026, the three inner layers of ITS are going to be replaced by a new vertex detector consisting of bent wafer-scale ultra-thin silicon sensors called Monolithic Stitched Active Pixel Sensors (MOSAIX). This will reduce the material budget close to the interaction point and improve the tracking precision and efficiency of the particles produced. The MOSAIX chips are currently under development. In parallel, a test system is being developed to test the MOSAIX chips. The test system must be done and ready for when the first MOSAIX chips are produced, in early 2025, to test the full functionality of the MOSAIX. This includes a large amount of data over 10.24 Gbps high speed channels, and a 5 Mbps control signal path. Alongside processing the large amount of output from the MOSAIX, the test system must generate stimuli to the whole MOSAIX chip. FPGAs allow us to incrementally design and test the test system, quickly adapting to any changes to the MOSAIX during development. A complex sensor needs a sophisticated test system. This posed several challenges. Some of the challenges include communication and signal parsing between many clock domains, high speed channels that can handle 10.24 Gbps communication, and a complex bus system with several masters. This test system also needs to be tested, and therefore a model of the MOSAIX is necessary to ensure the quality of the test system. This model is made in part using simpler models and modules extracted from the actual MOSAIX ASIC design. Since the MOSAIX is still under development, running adjustments must be made to the model. For this reason, FPGAs are an essential part of modeling. This talk will present the test system with its different modules, and how the challenges mentioned above were tackled. Furthermore, we will talk about the test setup of the test system and the making and testing of the MOSAIX model with the help of VHDL, UVVM, cocotb, and FPGAs.
UiO Yngve Hafting *Written: E, Oral: EoR*	**Experiences from teaching digital system design using Python-based testbenches** What is the key to using Python based testbenches in courses- or what do you need to understand to get started? - What did we do? (with example on displaying delta delays in simulation) - How did we fare? - What can others learn? - Will we continue using python?
Xiphera Matti Tommiska **Exhibitor** *Written: E, Oral: E*	**FPGA-Based Post-Quantum Secure Boot for Critical Computing Platforms** Building trust in semiconductor architectures is essential due to their critical information, extensive supply chains, and long product life cycles. Secure boot – that is, loading the operating system and other critical parameters in a trustworthy way – is the first step in the path for creating this trust. In today's landscape, where the development of quantum technology creates novel security threats, including Post-Quantum Cryptography (PQC) into the secure boot process is critical. In this presentation, we review how hardware-based cryptographic mechanisms can be used to secure the boot process of a computing platform. We will discover how the confidentiality, integrity, and authenticity of the boot process can be secured with post-quantum secure boot on FPGAs.

XJTAG Tommaso De Vivo **Exhibitor** *Written: E, Oral: E*	**Introduction to Accelerated PCBA Testing and Programming** Your FPGA board probably already has a JTAG connection, but did you know the interface also opens up the world of IEEE 1149.1 and 1149.6 boundary scan testing? The FPGA can help provide the solution to testing the complex PCBA it's part of, giving you an easy way to check for assembly faults across the board. It no longer matters if physical access is limited due to a lack of board space or the use of BGAs and other high-density packages because boundary scan effectively turns FPGA pins into virtual test probes. They can be electronically read and controlled through a JTAG connection, independent of the device's internal functionality and without configuring the device. It's not surprising that many engineers in all sectors, including automotive, medical, and defence are increasingly turning to boundary scan techniques to test their boards. Expensive functional board tests can be greatly simplified by using boundary scan to achieve much of the test coverage earlier in the production process. In fact, these tests can be used from prototype to manufacture and even across projects. This talk will introduce the technology and gives examples of how dedicated boundary scan test software can unlock the full capability of JTAG, providing you with an easy-to-use method to test and program boards.
Zolve Peter Uran *Written: E, Oral: E*	**Leveraging Pytest for HIL-testing: A quick start guide** *A quick start guide for making use of common Pytest features in the context of Hardware In the Loop testing*