FPGA
forum

FPGA-forum 2020

The 15th FPGA-forum – where the Norwegian FPGA community meets

- FPGA-forum and exhibition: Wednesday 12 and Thursday 13 February 2020

At Royal Garden Hotel (Trondheim)

FPGA-forum er den årlige møteplassen for FPGA-miljøet i Norge. Her samles FPGA-designere, prosjektledere, tekniske ledere, forskere, siste års studenter og de største leverandørene på ett sted for 2 dagers praktisk fokus på FPGA.

Det blir foredrag fra norske bedrifter om utviklingsmetodikk og praktisk erfaring, universitetene presenterer nye og spennende prosjekter, og leverandørene stiller med aktuelle tekniske innlegg med et minimum av markedsføring. På utstillingen vil du kunne vurdere teknologi, verktøy og tjenester fra de ledende aktørene i bransjen.

FPGA-forum byr i tillegg på en ypperlig anledning til å møtes og utveksle erfaring innenfor FPGA-miljøet i Norge - både i pausene og under det sosiale arrangementet på kvelden.

In English:

FPGA-forum is a yearly event for the Norwegian FPGA community. FPGA-designers, project managers, technical managers, researchers, final year students and the major vendors gather for a two-day focus on FPGA.

There will be presentations from the Norwegian industry about methodology and practical experience, - the universities will present new and exciting projects, and the vendors will have technical presentations with a minimum of marketing. At the exhibition, you can evaluate tools and technology from the leading vendors.

FPGA-forum also provides an excellent opportunity to meet and exchange experience with the Norwegian FPGA-community – during the breaks – and during the official dinner party on Wednesday.

Programme Wednesday, February 12, 2020 (Note: See appendix for abstracts)

(Flags show spoken language. Mixed means English on request. Slide language is normally the same as the title. If in doubt check appendix.)

09.00	Registration and coffee	
Session 1	**Track AB**	
09.25	**Opening** (by Jim Tørresen and Espen Tallaksen)	
09.30	**Keynote by Harry Foster, Chief Scientist Verification for the IC Verification Solutions division of Mentor, A Siemens Business** **'**FPGA Verification Maturity: A Quantitative Analysis' (Introduced by Arild Kjerstad, Kongsberg)	
10.30	**Vendor presentations** (3 min. per exhibitor - in alphabetical order – as per List of exhibitors (p5)	
11:10	**Coffee break (and exhibition)**	
Session 2	**Track A** Session chair: Jostein Ekre, Kongsberg Space Systems	**Track B** Session chair: Helge Fanebust, WideNorth
11.40	**Using FPGAs in power electronics at SINTEF energy** Kjell Ljøkelsøy, Sintef Energi	**A marriage – FPGA + Processor** Ed Garbett, Intel PSG (Arrow)
12:10	**The latest about probing** Thomas Göransson, 4Test / Keysight Technologies	**An overview of how new FPGA architectures and tools tries to support fast evolving application requirements** Jan Anders Mathisen, Avnet Silica (Xilinx)
12:40	**Prototyping of next-generation UPI node controller** Stein Kjølstad, Numascale	
13:10	**Lunch and Exhibition**	
Session 3	**Track A** Session chair: Svein Haustveit, HVL	**Track B** Session chair: Jim Tørresen, UiO
14:30	**Low-Cost, FPGA-based Generic Ultrasound Card** Trond Egil Gran, Embida	**Presentasjon av Masteroppgaver (For FPGA-forums pris for beste Masteroppgave 2019)** See 'Price award for Best FPGA related Master thesis in Norway' two pages further down.
15:00	**Functional Safety for FPGA designs** Stefan Bauer, Mentor, A Siemens Business	
15:30	**Addressing productivity of FPGA Development with Chisel** Øyvind Harboe, Zylin	
16:00	**Exhibition and Coffee**	
Session 4	**Track AB** Session chair: Jim Tørresen, UiO	
16:30	**Closing Keynote Day 1: Geir Førre, Firda** (og tidligere Chipcon, Energy Micro og Prox Dynamics) Bygge globalt ledende teknologiselskaper fra Norge	
17:15	**End of today's presentations**	
19.30	Aperitif, Royal Garden Hotel, Møterom Tavern	
20.00	Dinner party, Royal Garden Hotel. **Entertainment: Pirum**	

Programme Thursday, February 13, 2020 (Note: See appendix for abstracts)

(Flags show spoken language. Mixed means English on request. Slide language is normally the same as the title. If in doubt check appendix.)

Session 5	**Track A** Session chair: Øyvind Undstad, Kongsberg Spacetec	**Track B** Session chair: Kjetil Ullaland, UiB
09.00	**How you introduce RiscV into your FPGA design** David Esselius, Microchip Technology	**Adopting SystemVerilog for RTL as an IP company** Christian Grovdal, ARM
09:30	**Deep Learning: Going from unlabeled data to a trained network on a target** Daniel Aronsson, MathWorks	**Integration of Hardware Design Process in Web Based Requirement Management System** Yehoshua Shoshan, InnoFour
10:00	**Methodology - a must for complex FPGA design** David Clift, FirstEDA	**FPGA design av feilinjeksjonalgoritme for å emulere strålingsmiljø** Magnus Rentsch Ersdal, UiB
10:30	**Exhibition and Coffee**	
Session 6	**Track A.** Session chair: Hans Jørgen Fosse, Inventas	**Track B** Session chair: Oddgeir Austad, Kongsberg
11:00	**FPGA emulation for rapid development of next generation wireless SoCs** Helge Langen, Silicon Labs	**Onboard processing with reconfigurable computing on Small Satellites** Milica Orlandić, NTNU
11:30	**Take control of your Power integrity and power consumption** Thomas Göransson, 4Test / Keysight Technologies	**UVVM – All the new stuff** Espen Tallaksen, Bitvis
12:00	**Lunch and Exhibition**	
Session 7	**Track A** Session chair: Arild Kjerstad, Kongsberg	**Track B** Session chair: Knut Wold, NTNU
13:15	**BISMO: A Scalable Bit-Serial Matrix Multiplication Overlay for Reconfigurable Computing** Magnus Själander, NTNU	**Automated FPGA unit tests with Jenkins** Alf Storm, Nevion
13:45	**To 112Gbps and Beyond – A Transceiver technology update from Intel** Ed Garbett, Intel PSG (Arrow)	**Continuous integration: A practical approach to simultaneously compile and verify any number of FPGA designs in less than 60 minutes.** Geir Drange, PGS
14:15	**Coffee break**	
Session 8	**Track AB: Closing Keynotes** Session chair: Hans Jørgen Fosse	
14:45	**Closing Keynote Day 2: Eirik Evjen Hovstein, Maritime Robotics** Unmanned Systems and the unmanned industry	
15:30	**Closing Keynote Day 2: Espen Flo Eriksen, Kongsberg Defence and Aerospace** FPGA in Space Flight Hardware	
16:15	Closing words	
16:20	The end	

Keynotes:

- Opening keynote:
  Harry Foster, Chief Scientist Verification for the IC Verification Solutions division of Mentor, A Siemens Business
  'FPGA Verification Maturity: A Quantitative Analysis'

- Closing keynote Day 1:
  Geir Førre, Firda
  'Bygge globalt ledende teknologiselskaper fra Norge'
- Closing keynote Day 2:
  Eirik Evjen Hovstein, Maritime Robotics
  'Unmanned Systems and the unmanned industry'
- Closing keynote Day 2:
  Espen Flo Eriksen, Kongsberg Defence and Aerospace
  'FPGA in Space Flight Hardware'

Price award for Best FPGA related Master thesis in Norway:

FPGA-Forum's price is given to the best FPGA related Master thesis in Norway.

The award committee:

- **Dag Andreas Hals Samuelsen, University College of Southeast Norway (USN)**
- **Kjetil Ullaland, University of Bergen**
- **Hans Jørgen Fosse, Inventas**

The nominees in alphabetical order:

- **Dordije Boskovic:**
  Hardware implementation of a target detection algorithm for hyperspectral images
  Supervisors: Kjetil Svarstad and Milica Orlandic, Department of Electronic Systems, NTNU
- **Asbjørn Engmark Espe:**
  Real-Time Ray Tracing of Animated Sparse Voxel Octrees on FPGA
  Supervisors: Sverre Hendseth, Øystein Gjermundnes (ARM/NTNU),
  Department of Engineering Cybernetics, NTNU
- **Matias Gjestvang Greaker:**
  Development and Characterization of Readout Electronics for a Monolithic Active Pixel Sensor
  Supervisor: Ketil Røed, Department of Physics, University of Oslo
- **Edgar Mo Vedvik:**
  Implementing Data Cache Access Memoization (DCAM) in hardware to measure L1 DC and DTLB energy efficiency
  Supervisor: Magnus Själander, Department of Computer Science, NTNU

All four nominees will present their Master thesis in the last split session on day 1.
The winner will be announced during the dinner party.

List of exhibitors (for Wednesday and Thursday):

- 4Test www.4test.no
- Arrow Norway (Intel FPGA) www.intel.com/fpga
- Avnet Silica (Xilinx, MicroSemi) www.silica.no
- Inventas (Bitvis) www.bitvis.no
- FirstEDA (Aldec) www.firsteda.com
- InnoFour (Mentor) www.innofour.com
- MathWorks www.mathworks.com
- Nortelco Electronics www.nortelco.no
- Synective Labs www.synective.se

Entertainment (during the dinner party):

Pirum

FPGA-forum Program-committee:

- Arild Kjerstad, Kongsberg
- Hans Jørgen Fosse, Inventas
- Jan Anders Mathisen, Silica/Xilinx
- Jim Tørresen, University of Oslo
- Per Gunnar Kjeldsberg, NTNU
- Espen Tallaksen, Bitvis

Titles and Abstracts for presentations at FPGA-forum 2020

(In company alphabetical order)

Note that written and oral presentations may be in English or Norwegian. Some presenters may also switch to English on Request
Presentations are thus marked 'Written' or 'Oral' and E (English), N (Norwegian) or EoR (English on Request)

Company & Presenter	Title & Abstract
4Test / Keysight Technologies Thomas Göransson *Written: E, Oral: E*	**Take control of your Power integrity and power consumption** With todays fast switching devices, mutual dependence between the power rails and fast switching circuits and serial links will affect each other. Most electronics have one or more digital processing ICs, such as FPGAs or DSPs, that require multiple power-supply rails. There are various options to consider and potential pitfalls to avoid in powering these digital ICs. Having radio transmitters like in IOT devices the current will increase drastically and consideration from a power perspective needs to be taken. Which are the tools and the limitations on the different measurement approaches?
4Test / Keysight Technologies Thomas Göransson *Written: E, Oral: E*	**The latest about probing** The probe you connect will always be a part of your device under test, will it affect your measurement result? What are the challenges from DDR to high speed SERDES devices. Performance and flexibility will always be contradiction in probing. Tips and tricks to improve measurements results. How much bandwidth, loading is acceptable for my application.
Aldec	See FirstEDA
ARM Christian Grovdal *Written: E, Oral: E*	**Adopting SystemVerilog for RTL as an IP company** This presentation talks about how Arms GPU group went from Verilog to SystemVerilog for RTL development. As an IP provider, Arm is dependent on our RTL working in a wide array of tools from many different vendors. The presentation touches upon the challenges of the SystemVerilog language itself, how we evaluate and deploy new language construct and how we interact with the various tool vendors to ensure our RTL works everywhere.
Arrow	See Intel PSG
AvnetSilica (Xilinx) Jan Anders Mathisen *Written: E, Oral: N*	**An overview of how new FPGA architectures and tools tries to support fast evolving application requirements** Early FPGA's were considered improved glue-logic devices and then evolved to become essential building blocks in low-to-medium volume digital systems and systems requiring frequent updating. What requirements do current and future applications put on next generation FPGA/SoC architectures and supporting tools? How are these requirements addressed?
Bitvis Espen Tallaksen *Written: E, Oral: EoR*	**UVVM – All the new stuff** UVVM has been significantly updated through the European Space Agency's UVVM extension project. We have previously released the Scoreboard, and now lots of other new functionality has also been added. The most important of these are activity watchdog, Error injection, Monitor, Hierarchical VVCs and Specification Coverage. This presentation will go through all new features and explain how they will help you making a better testbench and develop this much faster.

Embida Trond Egil Gran *Written: E, Oral: N*	**Low-Cost, FPGA-based Generic Ultrasound Card** Embida has been working with different industrial ultrasound systems over the last years. Typically a SOC FPGA with a CPU running linux has been the main part of our systems. This is a flexible solution, but not suitable for many cases which require low power consumption and/or low cost. In systems made for EX zones where you are not allowed to consume much power, using several watts of power for the CPU makes the project very difficult since even finding an approved power supply is nearly impossible. In handheld devices you do not want a device that is too hot to hold. Our main workhorse over the last years has been the Intel Cyclone V SOC. For future systems we want to use something less power hungry which preferably can come at a lower cost. Unfortunately the main development of FPGAs lately has been on the high end side so currently as far as we know there is no replacement of the Cyclone V SOC that will give us any clear benefits. Our options are then the following: - Standalone CPU like the IMX8Mini with an FPGA. - FPGA with Soft Core CPU - Standalone MCU with and FPGA - Only FPGA no CPU or OS - Only one high end MCU (stm32h7 i.MX RT) We will present and discuss pros and cons for the various options
Firda Geir Førre *Written: N, Oral: N*	**Bygge globalt ledende teknologiselskaper fra Norge** Norge er et lite land med høyt kostnadsnivå og er ikke opplagt det beste stedet å bygge teknologiselskaper. Vi har samtidig erfart at det er fullt mulig gjennom kunnskap, kapital, fokus og aktivt lederskap. Det har ledet til vellykkede etableringer som Chipcon, Energy Micro og Prox Dynamics som alle har oppnådd å bli markedsledende innen sine ulike felt. Dette foredraget vil både komme inn på disse bedriftene og noen nye som vi for tiden jobber med gjennom se på hvordan har vi jobbet med bedriftsetableringene og hva vi anser som har vært viktig for å lykkes.
FirstEDA David Clift *Written: E, Oral: E*	**Methodology - a must for complex FPGA design** Increasing complexity In FPGA designs calls for a disciplined approach to verification. A sound methodology that can manage each abstraction level will ensure confidence to meet project deadlines and save unnecessary and expensive debug iterations. This presentation outlines a methodology utilising Jenkins as a project management tool, controlling a Xilinx based design running through early Design Rule Checking (DRC) to gate level verification using class leading tools from Sigasi and Aldec…
InnoFour Yehoshua Shoshan *Written: E, Oral: E*	**Integration of Hardware Design Process in Web Based Requirement Management (RM) System** Polarion ALM (Application Lifecycle Management) provide the frame to handle application from system specification to requirements to hardware bits (and software code) implementation, test and verification. There by it gives system architects, HW designers, project and product managers and other stake-holder a common ground to take best decisions with regards to priorities, content and cost. In the limited scope of this presentation, we will show the basic concepts of ALM and how they are implemented and impacting the design process – with emphasis on FPGA design.
InnoFour	See also Mentor
Intel PSG (Arrow) Ed Garbett *Written: E, Oral: E*	**A marriage – FPGA + Processor** Looking at options for efficiently connecting a processor and FPGA from embedded SoC internal connections to next generation standards like Compute Express Link CXL and PCIe Gen5 and everything in between. The presentation will look at the options and their advantages, at the end of the presentation you should have a better understanding about options for your next project.

Intel PSG (Arrow) Ed Garbett *Written: E, Oral: E*	**To 112Gbps and Beyond – A Transceiver technology update from Intel** A look at current and evolving transceiver technologies covering line rates from 1G to 112Gbps using NRZ and PAM4 line coding. During the presentation we will discuss the challenge of achieving a low bit error rate given extreme channel losses at the high data rates of 25Gbps and above, the need to move to PAM4 line coding and the advantages of using Forward Error Correction to build rock-solid links.
Kongsberg Defence and Aerospace Espen Flo Eriksen *Written: E, Oral: E*	***** Closing Keynote ***** **FPGA in Space Flight Hardware** Kongsberg Defence & Aerospace manufactures and delivers various types of electronics units for use in satellites and spacecraft. FPGA has been used to implement digital functionality in these products for several years and the talk will give an overview of this use. The complexity of functions implemented in FPGA has increased over time enabling a wide selection of functionality. Various space grade FPGA implementation technologies also enables different functions and products. The talk will give an overview of FPGA in space flight equipment up to the present day as well as thoughts and analysis of future use and possibilities for FPGA in this field.
Maritime Robotics Eirik Evjen Hovstein *Written: E, Oral: E*	***** Closing Keynote ***** **Unmanned Systems and the unmanned industry** Maritime Robotics is a leading provider of unmanned systems. They have delivered high class products and services with unmanned systems for the last 15 years, and will give us a brief introduction into the unmanned industry. The great development in electronics throughout the years has played an important role for the development of the industry and will still be for the future. Stay tuned for a journey into the unmanned industry both in the air, on the ground and on the water!
MathWorks Daniel Aronsson *Written: E, Oral: E*	**Deep Learning: Going from unlabeled data to a trained network on a target** This talk will cover the entire workflow for deep learning algorithm design, all the way from labelling data to designing and training networks, and finally deploying those networks to different targets. You will see how you can use interactive tools to speed up the labelling process, learn how to design deep learning-based vision applications like YOLO object detection, and how to re-target those applications to embedded CPUs and GPUs. To deploy the complete algorithm, code-generation tools are employed to automatically generate optimized code that can target embedded GPUs like the NVIDIA Drive PX2, Jetson TX2, and Jetson Xavier developer kits, Intel CPUs, and embedded ARM Cortex processors. The generated code is integrated with inference engines and libraries optimized for the chosen target platform.
Mentor, A Siemens Business Stefan Bauer *Written: E, Oral: E*	**Functional Safety for FPGA designs** Everybody is talking about and many companies are jumping on the functional safety train. The latest industry study from the Wilson Research Group shows, that almost half of the worldwide FPGA design projects are used within a safety application, i.e. autonomous driving or airplanes. Functional Safety is driving down risk of Electrical and Electronics malfunctioning due to failures. Standards like ISO 26262 or IES 61508 focus on two areas of faults: Systematic Faults and Random Faults. In this presentation Stefan Bauer, one of Mentor's verification experts, will give an introduction to functional safety standards and how to verify Malicious Faults, Systematic Faults and Random HW Faults.
Mentor, A Siemens Business Harry Foster *Written: E, Oral: E*	***** Opening Keynote ***** **FPGA Verification Maturity: A Quantitative Analysis** While multiple studies on IC/ASIC functional verification trends have been published, there have been no studies specifically focused on FPGA verification trends. To address this dearth of information, Harry presents the results from a recent large industry study on functional verification. The findings from this study provide invaluable insight into the state of today's FPGA market in terms of both design and verification trends. What is unique about this study is that for the first time the impact of this growing complexity has been quantified in terms verification effectiveness and effort.

Microchip Technology David Esselius *Written: E, Oral: E*	**How you introduce RiscV into your FPGA design** The Mi-V Ecosystem would support the designer for all stages in the development process. Much of the system functionalities of today adopted to be implemented into programable logic devices may not be parallel in nature. Using sequential preparation and computing within these devices are stretching the boundaries for what can be achieved in many aspects. Exhaustive synthesis and simulation run times also force the designs to be more configurable developed to reach system expectations.
Nevion Alf Storm *Written: E, Oral: EoR*	**Automated FPGA unit tests with Jenkins** Jenkins is an open source automation server for continuous integration and delivery. The presentation will describe a method to run a set of FPGA unit tests triggered by software repository changes and report the results. The overall solution as well as technical details will be presented.
NTNU Magnus Själander *Written: E, Oral: E*	**BISMO: A Scalable Bit-Serial Matrix Multiplication Overlay for Reconfigurable Computing** Matrix-matrix multiplication is a key computational kernel for numerous applications in science and engineering, with ample parallelism and data locality that lends itself well to high-performance implementations. Many matrix multiplicationdependent applications can use reduced-precision integer or fixedpoint representations to increase their performance and energy efficiency while still offering adequate quality of results. However, precision requirements may vary between different application phases or depend on input data, rendering constant-precision solutions ineffective. We present BISMO, a vectorized bitserial matrix multiplication overlay for reconfigurable computing. BISMO utilizes the excellent binary-operation performance of FPGAs to offer a matrix multiplication performance that scales with required precision and parallelism. We characterize the resource usage and performance of BISMO across a range of parameters to build a hardware cost model, and demonstrate a peak performance of 6.5 TOPS on the Xilinx PYNQ-Z1 board.
NTNU Milica Orlandić *Written: E, Oral: E*	**Onboard processing with reconfigurable computing on Small Satellites** A dramatic paradigm shift in the spacecraft development and mission concepts has moved towards miniaturization of satellite missions. To achieve significant reductions in dimensions, mass, development time and cost, there is a potential for technology development of a new generation of small satellites which exploits advances in modern technologies. The timing constraints, as well as data communication and storage constraints, that call for real-time on-board processing typically require the use of specialized hardware architectures. The emergence of programmable hardware devices such as Field Programmable Gate Arrays (FPGAs) can bridge the gap towards real-time onboard analysis of remote sensing data.
Numascale Stein Kjølstad *Written: E, Oral: E*	**Prototyping of next-generation UPI node controller** Numascale combines their knowledge of doing node controllers with state of the art Intel Xeon CPUs to build some of the most powerful shared memory systems. Numascale has been using FPGA prototyping as part of the design verification of the ASIC node controller. Numascale will share their lesson learned from the previous FPGA prototyping and present the plans for the next-generation ASIC node controller. The prototype for the next-generation node controller will consist of eight Neon-City servers, each holding two+FPGA processors. Eight multi-purpose FPGA boards holding a single Stratix10 size GX2800 FPGAs will be used to emulate the core functions of the node controller. The size and complexity of the next-generation node controller requires design partitioning into a multi-FPGA setup to be visited.
PGS Geir Drange *Written: E, Oral: E*	**Continuous integration: A practical approach to simultaneously compile and verify any number of FPGA designs in less than 60 minutes.** Continuous integration, as opposed to intermittent integration, is only really useful if the all the tasks involved in FPGA compilation and verification can be completed within a reasonable time after source code has been committed. 60 minutes is a reasonable time when considering that a developer should be able to make commits both before and after lunch. However, FPGA tool vendors seem to be stuck in the past both when it comes to tool flow and licensing, and this is a major challenge in CI for FPGA development. Compromises must be made, in particular when it comes to verification. This talk presents how PGS is using GitLab and GitLab Runners to compile, verify and release FPGA targets from Intel, Lattice and Xilinx, and where code sharing as a key principle.

Silicon Labs Helge Langen *Written: E, Oral: EoR*	**FPGA emulation for rapid development of next generation wireless SoCs** Silicon Labs' programmable, wireless devices are growing continuously larger and more complex, and contain an increasing number of peripherals and modules required to cooperate glitch-free up to the highest frequency supported by the chip. The embedded radio peripheral is one of the most complex, as it is subject to strict timing and power requirements in order to conform to the requirements set by protocols and regulations. An FPGA emulation platform that includes a working radio peripheral enables us to emulate new devices as accurately as possible. This makes it possible for digital design engineers, RF engineers and software developers to verify and test new products and assert design confidence prior to releasing the design for fabrication by the foundry. By doing this emulation, we can have a more rapid development of both hardware and software, as well as reduce the risk for costly respins.
Sintef Energi Kjell Ljøkelsøy *Written: E, Oral: EoR*	**Using FPGAs in power electronics at SINTEF energy** • Power electronics, introduction. • Sintef Energy, and the smartgridlab at NTNU/SINTEF. • Converter control using FPGAs. • Experiences.
UiB Magnus Rentsch Ersdal *Written: N, Oral: N*	**FPGA design av feilinjeksjonalgoritme for å emulere strålingsmiljø** ALICE Inner Tracking System (ITS) detektoren på CERN blir i disse dager oppgradert, og sensorelementene blir byttet ut med over 20 000 aktive piksel ICer kalt ALPIDE. ALPIDE chippene blir lest ut av 192 utlesningskort, der en Xilinx Kintex Ultrascale FPGA står for kontroll og utlesning av data. Dette utlesningskortet er plassert i et strålingsmiljø og det forventes derfor single event upsets (SEUs) i konfigurasjonsminnet til Xilinx FPGAen. På grunn av dette har det blitt designet et scrubbing nettverk bestående av et ekstern flashminne og en flashbasert Microsemi proAsic3 FPGA, som skal brukes til å korrigere disse feilene. For å kunne verifisere strålingstoleransen til designet på Xilinx FPGAen støtter også scrubbing løsningen muligheten for å gjøre feilinjeksjon i Xilinx konfigurasjonsminnet. Feilinjeksjonen foregår ved at tilfeldige bit i konfigurasjonsstrømmen blir flippet i sanntid i løpet av en scrubbing operasjon. Dette bidraget vil diskutere hvordan dette er løst i praksis, f eks. ved bruk av en pseudorandomgenerator designet i VHDL, men mulighet for å kunne kontrollere hvilket seed som blir gitt.
Xilinx	See also Avnet Silica
Zylin Øyvind Harboe *Written: E, Oral: E*	**Addressing productivity of FPGA Development with Chisel** Verilog and VHDL Verilog dates back to the early 80's and like the C programming language have not changed materially. Meanwhile, there has been innumerable software programming languages and concepts that have come and gone. There are new hardware programming languages that build on lessons learned in hardware and software to increase productivity, Chisel is one of those languages. In this presentation a few Chisel examples with test cases and FPGA P&R results are presented.