FPGA
forum

FPGA-forum 2019

The 14th FPGA-forum – where the Norwegian FPGA community meets

- FPGA-forum and exhibition: Wednesday 13 and Thursday 14 February 2019

At Royal Garden Hotel (Trondheim)

FPGA-forum er den årlige møteplassen for FPGA-miljøet i Norge. Her samles FPGA-designere, prosjektledere, tekniske ledere, forskere, siste års studenter og de største leverandørene på ett sted for 2 dagers praktisk fokus på FPGA.

Det blir foredrag fra norske bedrifter om utviklingsmetodikk og praktisk erfaring, universitetene presenterer nye og spennende prosjekter, og leverandørene stiller med aktuelle tekniske innlegg med et minimum av markedsføring. På utstillingen vil du kunne vurdere teknologi og verktøy fra de ledende leverandørene i bransjen.

FPGA-forum byr i tillegg på en ypperlig anledning til å møtes og utveksle erfaring innenfor FPGA-miljøet i Norge - både i pausene og under det sosiale arrangementet på kvelden.

In English:

FPGA-forum is a yearly event for the Norwegian FPGA community. FPGA-designers, project managers, technical managers, researchers, final year students and the major vendors gather for a two-day focus on FPGA.

There will be presentations from the Norwegian industry about methodology and practical experience, - the universities will present new and exciting projects, and the vendors will have technical presentations with a minimum of marketing. At the exhibition, you can evaluate tools and technology from the leading vendors.

FPGA-forum also provides an excellent opportunity to meet and exchange experience with the Norwegian FPGA-community – during the breaks – and during the official dinner party on Wednesday.

Programme Wednesday, February 13, 2019 (Note: See appendix for abstracts)

09.00	Registration and coffee	
Session 1	**Track AB**	
09.25	**Opening** (by Jim Tørresen and Espen Tallaksen)	
09.30	**Keynote by Ted Speers,** **Head of Product Architecture and Planning, Technical Fellow at Microchip Technology Inc.** 'RISC-V and the Future of Computing' (Introduced by Arild Klerstad)	
10.30	**Vendor presentations** (3 min. per exhibitor - in alphabetical order)	
11:10	**Coffee break (and exhibition)**	
Session 2	**Track A** Session chair: Svein Haustveit, HVL	**Track B** Session chair: Trude Støren, Embida
11.40	**FPGA, siste valget** Tore Fleten, Cisco	**High Level Tools for Rapid Prototyping and Early Verification in FPGA and SoC Design – How good are they really?** Jonas Rutström, MathWorks
12:10	**CAN bus in ALICE ITS Upgrade Readout Electronics and UVVM CAN bus BFM** Simon Voigt Nesbø, HVL	**System On Modules – With FPGA's** Nikolay Rognlien, Arrow (Intel FPGA)
12:40	**Lunch and Exhibition**	
Session 3	**Track A** Session chair: Tore Eide, Inventas	**Track B** Session chair: Hans Jørgen Fosse, Vitoteq
14:00	**EMC in an environment with high speed serial links and the challenges with high dynamic power delivery in IOT devices** Thomas Göransson, 4Test / Keysight Technologies	**Embedding Machine Learning in FPGA's** Jan Anders Mathisen, AvnetSilica (Xilinx)
14:30		**Optimized Deep Learning on FPGAs** Yasser Bajwa, Grazper
15:00	**Why fast feedback makes you a better designer and tester** Hendrik Eeckhaut, Sigasi	**Graphcore Intelligence Processing unit (IPU) – scaleout system for artificial intelligence and machine intelligence** Morten Schanke, Graphcore
15:30	**Exhibition and Coffee**	
Session 4	**Track A** Session chair: Johan Alme, UiB	**Track B** Session chair: Jim Tørresen, UiO
16:00	**Portable Stimulus for SystemVerilog UVM, VHDL UVVM, and C-based Verification Environments (60 min)** Stefan Bauer, Mentor, A Siemens Business	**Presentasjon av Masteroppgaver** **(For FPGA-forums pris for beste Masteroppgave 2018)**
16:30		
17:00	**End of today's presentations**	
19.30	Aperitif TBD, Royal Garden Hotel	
20.00	Dinner party, Royal Garden Hotel. Entertainment: Roar Brekke, Stand-up comedian	

Programme Thursday, February 14, 2019 (Note: See appendix for abstracts)

Session 5	**Track A** Session chair: Kjetil Svarstad, NTNU	**Track B** Session chair: Knut Wold, NTNU
09.00	**Efficient use of FPGA resources in CNNs** Sigurd Øyen, Embida	**FPGA Emulation used in CMOS Image Sensor Design** Petter Gustad, Omnivision
09:30	**Deep Learning Inference on FPGA** August von Hacht, Synective	**Design of External Scrubber for a Xilinx Ultrascale FPGA** Magnus Rentsch Ersdal, UiB
10:00	**FPGA – The Future of Multifunction Accelerators** DJ Gianduso (Intel FPGA)	**Dolphicam2: Ultrasound camera using multiple FPGAs** Øystein Knauserud, Dolphitech
10:30	**Exhibition and Coffee**	
Session 6	**Track A.** Session chair: Helge Fanebust, WideNorth	**Track B** Session chair: Arild Kjerstad, Kongsberg
11:00	**Challenges of 56G and beyond serial data transfer.** David Taylor, Xilinx	**Continous Integration and Testing for FPGA Development - -Experience from 3 years of practical day-to-day use** Øyvind Riis, Appear TV
11:30	**FPGA and Software Defined Radios (SDR) -- Generic platform for collecting and transmitting sensor data** Tom Morten Berge UiO	**VHDL Verification and UVVM - for beginners** Espen Tallaksen, Bitvis
12:00	**Lunch and Exhibition**	
Session 7	**Track A** Session chair: Øystein Gjermundnes, ARM	**Track B** Session chair: Tore Fleten, Cisco
13:15	**FPGAs versus processors in crypto implementation** Matti Tommiska, Xiphera	**Design and Implementation of a High-Rate Turbo Decoder.** Øyvind Undstad, Kongsberg (KDA)
13:45	**SysML modellering av FPGA** Geir Åge Noven, Kongsberg (KDA)	**VHDL Assertions – for beginners** Espen Tallaksen, Bitvis
14:15	**Coffee break**	
Session 8	**Track AB: Closing Keynotes** Session chair: Jim Tørresen og Per Gunnar Kjeldsberg	
14:45	**Closing Keynote: Bernt Øivind Børnich, Halodi Robotics** Cost driven development of a humanoid robot for mass production	
15:30	**Closing Keynote: Egil Eide, 3D-radar** There and Back again	
16:15	Closing words	
16:20	The end	

Keynotes:

- Opening keynote:
  Ted Speers, Head of Product Architecture and Planning, Technical Fellow at Microchip Technology Inc.
  'RISC-V and the Future of Computing'

- Closing keynote Day 2:
  Bernt Øivind Børnich, Halodi Robotics
  'Cost driven development of a humanoid robot for mass production'
- Closing keynote Day 2:
  Egil Eide , 3D-radar
  'There and Back again'

Price award for Best FPGA related Master thesis in Norway:

FPGA-Forum's price is given to the best FPGA related Master thesis in Norway.

The award committee:

- Dag Andreas Hals Samuelsen, University College of Southeast Norway (USN)
- Kjetil Ullaland, University of Bergen
- Hans Jørgen Fosse, Vitoteq

The nominees in alphabetical order:

- Johan Austlid Fjeldtvedt, NTNU
  Supervisors: Kjetil Svarstad and Milica Orlandic
  'Efficient Streaming and Compression of Hyperspectral Images'
- Youri Vassiliev, NTNU (Erasmus utveksling)
  Supervisors: Kimmo Kansanen
  'FPGA implementation of an efficient high-speed DVB-S2X block-interleaver'

Both nominees will present their Master thesis in the last session on day 1.
The winner will be announced during the dinner party.

One Workshop/Tutorial/Seminars Day 0, Tuesday 12th:

Generating GPU-code from MATLAB for desktop and embedded targets

Organiser: MathWorks

Location: Radisson Blu Royal Garden. Room: Sverresborg

Time: Tuesday, February 12: 10:00–15:45

Presenter: Jonas Rutström

Cost: Free

Please note: You need to bring your own laptop. We will provide you with licenses to use during the workshop.

Attendance is limited so register now by providing your email address.

In this workshop, you will learn how to generate CUDA code from MATLAB to run on Nvidia desktop and embedded GPUs. MATLAB is the ideal environment for exploring, developing and prototyping algorithms. GPUs are the hardware of choice for many applications, such as signal, image processing and deep learning, that benefit from the parallel processing they offer. GPU Coder now offers a route to transition from MATLAB development to deployment on GPU via the generation of CUDA code.

The workshop is suitable for engineers with experience in MATLAB with a need to deploy algorithms to GPU for acceleration or implementation. Knowledge of CUDA and/ or GPU architectures is not required, but may be useful.

Through hands-on exercises you will experience how these techniques help you make better design decisions for highly parallel processing.

- Run MATLAB algorithms directly on the GPU via gpuArray
- Prototype and accelerate implementations with automatic CUDA code generation
- Enhance throughput through design patterns optimized for GPU architecture
- Generate CUDA from deep learning networks for acceleration and implementation
- Deploy generated code to desktop and embedded GPUs

For a detailed agenda and registration please visit this page.

List of exhibitors (for Wednesday and Thursday):

- 4Test www.4test.no
- Arrow Norway (Intel FPGA) www.intel.com/fpga
- Arrow Norway (Microchip) www.microchip.com
- Avnet Silica (Xilinx) www.silica.no
- BitSim www.bitsim.com
- Bitvis www.bitvis.no
- Embida www.embida.no
- FirstEDA with Sigasi www.firsteda.com
- Innofour (Mentor) www.innofour.com
- MathWorks www.mathworks.com
- Synective Labs www.synective.se

Entertainment (during the dinner party):

Roar Brekke – An experienced entertainer and stand-up comedian meets experienced designers

With more than more than 20 years of experience from entertainment, the stand-up event during our dinner (some in English and some in Norwegian) is well tested and should bring our mood to new heights. (http://www.roarbrekke.no)

FPGA-forum Program-committee:

- Arild Kjerstad, Kongsberg
- Hans Jørgen Fosse, Vitoteq
- Jan Anders Mathisen, Silica/Xilinx
- Jim Tørresen, University of Oslo
- Per Gunnar Kjeldsberg, NTNU
- Espen Tallaksen, Bitvis

Titles and Abstracts for presentations at FPGA-forum 2019

(In company alphabetical order)

Note that written and oral presentations may be in English or Norwegian. Some presenters may also switch to English on Request
Presentations are thus marked 'Written' or 'Oral' and E (English), N (Norwegian) or EoR (English on Request)

Company & Presenter	Title & Abstract
3D-radar Egil Eide *Written: E, Oral: E*	***** Closing Keynote ***** **There and Back again** Egil Eide, founder of 3d-Radar and associate professor at NTNU Department of Electronic Systems tells the story about 3d-Radar AS from the startup in 2001, the growth phase and acquisition by Curtiss-Wright and Chemring around 2010, to the re-acquisition by the founders in 2018. 3d-Radar manufactures advanced ground penetrating radars for mapping underground utility structures and subsurface infrastructure. From being literally under the radar for several years, 3d-Radar's products have now become well recognized as a standard tool for the growing market for highway and bridge deck inspection.
4Test / Keysight Technologies Thomas Göransson *Written: E, Oral: E*	**EMC in an environment with high speed serial links and the challenges with high dynamic power delivery in IOT devices** (60 min) With increasing data rate and complexity in high speed digital systems, this presentation will focus on the wider picture with dependence between Electromagnetic Compatibility, Signal Integrity and Power Integrity. Having fast edges and power supply coupling in to each other and the ambient environment. Electromagnetic compatibility(EMC) test is not something companies do in the end of the development cycle. This need to be considered earlier in the project with pre-compliance test together with signal integrity and power integrity analysis. The sources of jitter also will be affecting EMC. We will also cover the challenges to measure a dynamic current drain at wireless devices operating in high dynamic current and frequency, from, nA-mA(1:1000000) at frequency's, DC-MHz(1:10000000)for battery consumption in especially IOT devices. Modern applications with FPGA's on a circuit board easily can have 15 power supplies, multiple high-speed SerDes type of digital interfaces, as well as the DDR4 and its multi-layer PCB. All these interfaces can interfere with each other. If this crosstalk can be discovered and corrected early there will be a better chance to pass the EMC test. Limitations with different measurement methods will be covered.
Aldec	See FirstEDA
Appear TV Øyvind Riis *Written: E, Oral: E*	**Continous Integration and Testing for FPGA Development - -Experience from 3 years of practical day-to-day use** Appear TV has been using a CI for its FPGA development for the last three years. We will present our system for automating VHDL compilation, VHDL simulation, FPGA build and FPGA regression test. We will also give examples of issues and challenges which we have encountered and give some recommendations and guidelines for others who want to use CI for FPGA development.
Arrow (Intel FPGA) Nikolay Rognlien *Written: E, Oral: EoR*	**System On Modules – With FPGA's** FPGAs can be difficult and costly to integrate on your own custom pcb. System On Modules can address many of the challenges you may face for your new projects. This session will focus on the benefits of SoMs and how to choose the right one from the growing portfolio of modules.

AvnetSilica (Xilinx) Jan Anders Mathisen *Written: E, Oral: N*	**Embedding Machine Learning in FPGA's** Recent developments in Machine Learning have shown promising results when implemented in FPGAs and MPSoCs. The presentation will give an overview of ML and its implementation in FPGAs and MPSoCs – including a look at tool flows and results.
Bitvis Espen Tallaksen *Written: E, Oral: E*	**VHDL Verification and UVVM - for beginners** There is a huge efficiency and quality potential in making good and well-structured testbenches. This applies to most developers and most companies. Improvement here is actually quite easy and does not require any investment at all. In fact – if you do this right – you will save time and improve quality already in your first project. This presentation will show you how to get started and what you should do – independent of tools and methodologies, but using examples from UVVM Utility Library Note: This presentation is *not* intended for designers who already knows UVVM Utility Library
Bitvis Espen Tallaksen *Written: E, Oral: E*	**VHDL Assertions – for beginners** There is a lot of talk about assertions – both in testbenches and directly in the design. These assertions could be very useful in order to save time and improve quality. Some very important benefits of assertions are: - Reduce debug time, by detecting problems and bugs where they occur, and not later - on the outputs - Check assumptions - Avoid wrong integration of a module - Avoid illegal software control This presentation will briefly mention assertions in SVA, PSL and OVL, and primarily focus on how assertions can be applied and coded in VHDL.
Cisco Tore Fleten *Written: N, Oral: N*	**FPGA, siste valget** Hvor står vi etter tiår med FPGA forum, hvor FPGA er blitt rost opp i skyene? Gang på gang får vi høre hvor fantastisk FPGA er og hvor mye den kan brukes til. Allikevel blir FPGA sett på som et nødvendig onde og siste valg når nye produkter skal utvikles. Denne presentasjonen vil ta for seg noen av de innarbeidede tankene (true or false) om FPGA.
Dolphitech Øystein Knauserud *Written: E, Oral: E*	**Dolphicam2: Ultrasound camera using multiple FPGAs** Dolphicam2 is an ultrasound camera used for Non-Destructive Testing. This talk will briefly present the ultrasound technology and why we developed Dolphicam2. The system has two FPGA's and the presentation will discuss how we decided which FPGA's we chose, system architecture and design flow. Further the presentation will show how we implemented this multiple-FPGA design in Dolphicam2 and the challenges we met during the process.
Embida Sigurd Øyen *Written: E, Oral: N*	**Efficient use of FPGA resources in CNNs** Often are FPGAs used as a hardware accelerator in bigger systems. When implementing the entire inference part of a CNN in an FPGA, how can you efficiently reuse the available resources with the changing dimensions of the CNN?

Graphcore Morten Schanke *Written: E, Oral: EoR*	**Graphcore Intelligence Processing unit (IPU) – scaleout system for artificial intelligence and machine intelligence.** The Graphcore Intelligence Processor Unit (IPU) is a completely new processor design that has been developed from the ground up to work efficiently with machine learning algorithms and be used in scale-out systems. Its architecture has been specifically developed to tackle the extremely complex, high-dimensional models needed by machine intelligence solutions. The Graphcore IPU processor is ideally suited to scaling and directly addresses the key requirements to enable IPU-Rackscale systems that could deliver 100x or 1000x more AI compute than current systems. This will allow developers to solve machine learning problems that are currently impossible and massively reduce problem solving times. Machine Intelligence requires a completely new approach for scale-out fabrics. The IPU´s innovative use of the Bulk Synchronous Parallel (BSP) computation model - well known in the HPC and parallel compute worlds - provides a key foundation for building Machine Intelligence Rackscale systems with 1000s of IPU's. Fabric-based MI workload acceleration is another key element, as well as an ability to on-demand elastically pool IPUs into secure domains.
Grazper Yasser Bajwa *Written: E, Oral: E*	**Optimized Deep Learning on FPGAs** FPGAs offer several advantages for use in the field of deep learning in terms of power, stability and performance. However, current frameworks sacrifice considerable performance in favour of flexibility when used for FPGAs. The presentation deals with the advantages of implementing deep convolutional networks that are specifically designed for FPGAs. It does so by outlining methods for optimally using the FPGA resources by employing techniques such as bit-width reduction and 1-bit weights.
Halodi Robotics Bernt Øivind Børnich *Written: E, Oral: E*	***** Closing Keynote ***** **Cost driven development of a humanoid robot for mass production** In a domain where you typically either deliver sub components or integrate them, we take a holistic approach to developing a highly complex mechatronics system for mass production.
HVL Simon Voigt Nesbø *Written: E, Oral:EoR*	**CAN bus in ALICE ITS Upgrade Readout Electronics and UVVM CAN bus BFM** For the Long Shutdown 2 (LS2) upgrade of the ALICE experiment at the LHC, the Inner Tracking System (ITS) of the experiment will be completely replaced with a new design. The new design consists of 24 120 pixel chips, organized in 7 cylindrical layers located directly around the experiment's collision point. Data from the pixel chips are read out using 192 Readout Unit (RU) boards, and shipped off the boards using optical links. The board has a Xilinx UltraScale FPGA for the datapath, trigger distribution, and most of the board's control systems. Control and monitoring of the boards is also performed using the optical links, under normal operation. But as a backup system, a CAN bus interface is also provided by the boards, which allows for the same control and monitor options. This talk will present the implementation of CAN bus and a High Level Protocol used by the RU, and also a Bus Functional Model (BFM) for CAN bus developed for the UVVM framework.
Innofour	See Mentor Graphics
Intel FPGA	See also Arrow
Intel FPGA DJ Gianduso *Written: E, Oral: E*	**FPGA – The Future of Multifunction Accelerators** We're living in an increasingly smart and connected world. A world that is generating increasing amounts of data and we are driven to find new ways to extract value from this data. The world needs technology solutions that can not only meet today's demands but also tomorrows. FPGAs are stepping up to meet this challenge by writing the next chapter in the story of their evolution – FPGA as a reconfigurable multifunction accelerator. What are the characteristics of this new chapter, what are the strategies the FPGA industry is deploying to address the demand?

Kongsberg (KDA) Geir Åge Noven *Written: E, Oral: EoR*	**SysML modellering av FPGA** SysML er et grafisk modelleringsspråk (som UML), som er tatt i bruk av KDA for å systematisere design av FPGA i en tidlig fase. Den grafiske syntaksen kan brukes til å beskrive interfacer, struktur og oppførsel av (VHDL)pakker og arkitekturer/entiteter. Den kan også brukes til å definere krav og spore disse til designenheter. KDA har brukt den resulterende objektdatabasen til automatisk generering av entiteter og strukturell kode, i tillegg til beskrivende dokumentasjon. Presentasjonen beskriver metodikken og viser eksempler på SysML syntax og genererte filer.
Kongsberg (KDA) Øyvind Undstad *Written: E, Oral: Eor*	**Design and Implementation of a High-Rate Turbo Decoder.** Kongsberg Spacetec AS has developed a high data rate SCCC-decoder for data rates up to 2.7 Gbps under ESA's GSTP program. SCCC (Serial Concatenated Convolutional Code) is part of a class of forward error correction FEC codes popularly called turbo codes. Decoding SCCC is an iterative process requiring a large amount of computation. The presentation will go through some of the challenges we had to overcome in order to meet the requirements.
MathWorks Jonas Rutström *Written: E, Oral: E*	**High Level Tools for Rapid Prototyping and Early Verification in FPGA and SoC Design – How good are they really?** High level tools for HDL design and verification has gained a lot of attention over the last couple of years. It is claimed that they increase the productivity of engineering teams all over the world allowing them to spend their precious time on things that really matters in combination with a superior workflow to detect design errors and get rid of manual coding errors. But – really, is this something that you should adopt in your design workflow? In this presentation we'll walk you through a real-world example of how development time was reduced in the development of an FPGA-Controlled Surgical Instrument. We hope to inspire you to investigate new powerful solutions that take you and your colleagues into the next level of product development
Microchip Technology Ted Speers *Written: E, Oral: E*	***** Opening Keynote ***** **RISC-V and the Future of Computing** A useful way to look at a computer system is to view it an organism comprised of nerve endings (devices, sensors and actuators), nerves (gateways and transport) and the brain (data centers and the cloud). We've gone through at least three major stages of evolution of this organism, starting with telephony and moving to computing and then mobile. In this talk, we'll review how this system has evolved, how value was captured at each stage of evolution and project how this system is poised to evolve in the post Moore's Law era and the role that the RISC-V ISA will play in that evolution.
Mentor, A Siemens Business Stefan Bauer *Written: E, Oral: E*	**Portable Stimulus for SystemVerilog UVM, VHDL UVVM, and C-based Verification Environments (60 min)** The Portable Test and Stimulus Standard (PSS) defines a specification to create abstract, easily-reusable representations of stimulus and test scenarios. When using PSS, a single description of the verification intent is defined and the tool generates reusable scenario-level stimuli retarget-able across simulation, emulation, and other verification targets. Using PSS creates higher quality tests, controls repetition and redundancy, and results in 10X faster achievement of target coverage. In this presentation, Stefan Bauer, one of Mentor's verification experts, will introduce this new standard and show how PSS can be used to generate scenario-level tests for SystemVerilog UVM, VHDL UVVM, and even C-based verification environments from a single abstract model.
Omnivision Petter Gustad *Written: E, Oral: E*	**FPGA Emulation used in CMOS Image Sensor Design** A short introduction to CMOS image sensor technology and how FPGA emulation can be used during development and verification. The emulator contains a synthesizable model of the pixel array output signals, analog/digital conversion, and random temporal and fixed pattern noise sources. This acts as stimuli to the image signal processing block and output data path of the chip.

Sigasi Hendrik Eeckhaut *Written: E, Oral: E*	**Why fast feedback makes you a better designer and tester** In digital design and verification you continuously get into this typical feedback loop: First you write some code, you verify it behaves as you intended and next you need to modify some more code to make sure it does, and so on. This loop, again and again slows you down. You spend a lot of time waiting for feedback. You have a lot of context switches, which drain your mental energy and have a serious impact on the quality of your work. So ultimately you end up with low productivity. In this presentation we will discuss techniques to get faster feedback during your design and verification work. Paramount is automation: make sure your tools and processes are automated. In addition, you need automated tools to present you with the feedback (both text and graphics) in a fast and clear way. Depending on the activity (design, simulation, formal verification, synthesis ...) "fast" will have a different time scale, but the same principles apply. When you speed up the feedback loop: you will spend less time waiting; you will have less context switches and hence better focus; you will have higher quality code in a short time; you will be more productive and feel more satisfied about your work.
Synective August von Hacht *Written: E, Oral:E*	**Deep Learning Inference on FPGA** Utilizing deep learning inference in smaller embedded devices will enable a large range of new applications. But deep learning inference typically requires massive hardware accelerations, something which the FPGA may offer. The key aspect of the FPGA is the possibility to obtain a low power implementation based on an architecture supporting smaller bit sizes and efficient hardware reuse. However, in order to obtain such an implementation, the problem of designing an efficient shuffling of parameter data to the inference engines has to be solved. This talk will highlight this challenge and present two inference implementations for real time image processing using deep neural networks.
UiB Magnus Rentsch Ersdal *Written: E, Oral: E*	**Design of External Scrubber for a Xilinx Ultrascale FPGA** This talk presents the external scrubber solution for the Xilinx Ultrascale FPGA on the Readout Unit board of the upgraded ALICE Inner Tracking System (ITS) Detector at CERN. In the context of FPGAs, scrubbing is a technique that is used to correct errors in the configuration memory array by overwriting the memory content. Xilinx offers the internal SemIP solution for this, but the solution had some limitations which made it undesirable for use in the ITS Readout Unit. The external scrubbing solution consists of a Microsemi ProAsic3 Flash-based FPGA and a Samsung Flash Memory device, and performs the scrubbing using the SelectMap interface. The design is implemented with local triple modular redundancy and supports ECC encoded bitstreams on the flash device for initial configuration and blind scrubbing, as well as the possibility to do fault injection from software. Combined with the firmware design for the Xilinx Ultrascale, which also employs radiation mitigation techniques and triplicated logic, the failure rate due to radiation will be negligible for the ITS Readout Unit.
UiO Tom Morten Berge *Written: E, Oral: E*	**FPGA and Software Defined Radios (SDR) -- Generic platform for collecting and transmitting sensor data** SDRs are integrated radio solution programmable by software, which makes it highly flexible with support for wide frequency range, modulation bandwidth and integrated ADC/DACs. Together with an Altera FPGA, a generic platform has been created to collect sensor data and transmit. The platform contains both analog and digital interfaces for collecting sensor data, encoded in the FPGA before transmitted by the SDR. The platform has been developed to be used as a sensor platform for the 4DSPACE program at University of Oslo which investigates plasma instabilities in the upper atmosphere. However, it's generic nature makes it possible to be used by a wide range of projects.
Xilinx David Taylor *Written: E, Oral: E*	**Challenges of 56G and beyond serial data transfer.** Xilinx will provide an in depth insight to instruct and advise potential adopters of this exciting and challenging new technology.
Xilinx	See also Avnet Silica

Xiphera Matti Tommiska *Written: E, Oral: E*	**FPGAs versus processors in crypto implementation** Building a secure system requires implementations of cryptographic algorithms and protocols. In embedded systems, a designer has two main options: a software implementation running on a microprocessor/controller or a hardware implementation, most typically, with an FPGA. In this talk, we analyze the differences of FPGA- and microprocessor/controller -based cryptography implementations from three points of view: security, performance, and implementability. Security is not only about selecting secure cryptographic algorithms and protocols, but also the implementations themselves must withstand attacks targeting implementation-level weaknesses. FPGAs have robust advantages in security designs -- for example, critical security functions can be isolated and fine-grained control over a design allows for advanced countermeasures against implementation attacks. Performance in terms of latency, throughput, power or energy consumptions, etc. are often significantly better with FPG- based cryptography, and several tens of Gbps encryption/decryption speeds can be reached with relatively modest resources in modern FPGAs. The traditional advantage of software has been ease of implementability, as cryptographic libraries are widely available and quite straightforward to integrate with the rest of the system. However, the situation with FPGAs is not much different due to the availability of third-party IP blocks.