FPGA forum

Final programme

FPGA-forum 2018

The 13th FPGA-forum – where the Norwegian FPGA community meets

- FPGA-forum and exhibition: Wednesday 14 and Thursday 15 February 2018
- Tutorials/Workshops: Tuesday 13 February 2018

At Royal Garden Hotel (Trondheim)

FPGA-forum er den årlige møteplassen for FPGA-miljøet i Norge. Her samles FPGA-designere, prosjektledere, tekniske ledere, forskere, siste års studenter og de største leverandørene på ett sted for 2 dagers praktisk fokus på FPGA.

Det blir foredrag fra norske bedrifter om utviklingsmetodikk og praktisk erfaring, universitetene presenterer nye og spennende prosjekter, og leverandørene stiller med aktuelle tekniske innlegg med et minimum av markedsføring. På utstillingen vil du kunne vurdere teknologi og verktøy fra de ledende leverandørene i bransjen.

FPGA-forum byr i tillegg på en ypperlig anledning til å møtes og utveksle erfaring innenfor FPGA-miljøet i Norge - både i pausene og under det sosiale arrangementet på kvelden.

In English:

FPGA-forum is a yearly event for the Norwegian FPGA community. FPGA-designers, project managers, technical managers, researchers, final year students and the major vendors gather for a two-day focus on FPGA.

There will be presentations from the Norwegian industry about methodology and practical experience, - the universities will present new and exciting projects, and the vendors will have technical presentations with a minimum of marketing. At the exhibition, you can evaluate tools and technology from the leading vendors.

FPGA-forum also provides an excellent opportunity to meet and exchange experience with the Norwegian FPGA-community – during the breaks – and during the official dinner party on Wednesday.

Programme Wednesday, February 14, 2018 (Note: See appendix for abstracts)

09.00	Registration and coffee	
Session 1	**Track AB -** Session chair: Per Gunnar Kjeldsberg, NTNU	
09.25	**Opening** (by Jim Tørresen and Espen Tallaksen)	
09.30	**Keynote by Craig Davis,** **Senior Product Marketing Manager, Intel Programmable Solutions Group** 'Accelerating a Smart and Interconnected World'	
10.30	**Vendor presentations** (3 min. per exhibitor - in alphabetical order)	
11:10	**Coffee break (and exhibition)**	
Session 2	**Track A** Session chair: Johan Alme, UiB	**Track B** Session chair: Per Gunnar Kjeldsberg, NTNU
11:40	**Mastering Clock Domain Crossing challenges in FPGA Design** Stefan Bauer, InnoFour (Mentor Graphics)	**FPGA-based compute acceleration – local systems and cloud based services** Jan Anders Mathisen, AvnetSilica (Xilinx)
12:10	**Dealing with CDC verification complexity in large-scale FPGA designs** Sergei Zaychenko, Aldec	
12:40	**Lunch and Exhibition**	
Session 3	**Track A** Session chair: Torstein Dybdahl, Acapo AS	**Track B** Session chair: Bjørn B. Larsen, NTNU
14:00	**Godkjenning av missil med sikkerhetskritiske FPGAer** John Aasen, Kongsberg	**Essential tool for FPGA board bring up.** Nikolay Rognlien, Arrow (Intel FPGA)
14:30	**Secure FW upgrade of embedded systems** Svein M Birkemoe, Hiddn	**FPGA in Neuroscience** Lars Forsberg, Synective Labs
15:00	**Exhibition and Coffee**	
Session 4	**Track A** Session chair: Arild Kjerstad, Kongsberg	**Track B** Session chair: Jim Tørresen, UiO
15:30 **16:00**	**Skyrocket FPGA team productivity with templates and standardized IP interfaces** Rune Bæverud, Thales	**Presentasjon av Masteroppgaver** **(For FPGA-forums pris for beste Masteroppgave 2017)**
16:30	**Exhibition and Coffee?**	
Session 4x	**Track AB** Session chair: Hans Jørgen Fosse, Vitoteq	
16:45	**Closing Keynote by Marius Fraurud, VP R&D, Tomra** 'The story of TOMRA. From a small Norwegian start-up to a large international company with a global footprint.	
17:30	**End of today's presentations**	
19.30	Aperitif, Royal Garden Hotel	
20.00	Dinner party, Royal Garden Hotel. Entertainment: Candiss	

Programme Thursday, February 15, 2018 (Note: See appendix for abstracts)

Session 5	**Track A** Session chair: Kjetil Svarstad, NTNU	**Track B** Session chair: Knut Wold, NTNU
09.00	**Hva er deep learning? Og hvorfor er FPGA relevant?** Robert Engels, Acando	**High-Speed Software Defined Radio -- Generic high-speed broadband SDR platform implemented in FPGA using direct sampling at L-band** Jean Bruant, WideNorth
09:30	**Embedded GPUs: Compiling high-level vision and deep learning algorithms** Daniel Aronsson, MathWorks	**A low-power, full duplex, controlled spectrum modem link for single twisted pair power+communication applications** Geir Drange, PGS
10:00	**Accelerate FPGA development times with Intel's HLS compiler – a tutorial** Nikolay Rognlien, Arrow (Intel FPGA)	**IOT from a power perspective** Thomas Gøransson, 4Test / Keysight Technologies
10:30	**Exhibition and Coffee**	
Session 6	**Track A.** Session chair: John Aasen, Kongsberg	**Track B** Session chair: Arild Kjerstad, Kongsberg
11:00	**Erfaringer med Vivado HLS for design av FPGA signalprosesseringskjede - C-design og testbenker** Ole Henrik Waagaard, Alcatel Submarine Networks Norway	**Mi-V: a RISC-V based ecosystem – who needs another soft processor?** Anders Hillström, MicroSemi
11:30	**Erfaringer med Vivado HLS for design av FPGA signalprosesseringskjede - HLS fra en vhdl designers perspektiv** Dag K. W. Rognlien	**Python – What's the question?** Jørgen Linnerud, Cisco Systems Norway
12:00	**Lunch and Exhibition**	
Session 7	**Track A** Session chair: Svein Haustveit, HVL	**Track B** Session chair: Arild Kjerstad, Kongsberg
13:15	**Mellom vitskap og handverk - ingeniørutdanning for framtida.** Lars Lundheim, NTNU	**FPGA in RIMFAX - a ground penetrating radar for NASA's Mars-2020 mission** Sverre Brovoll, FFI
13:45	**Produktutvikling i grensesnittet elektronikk, mekanikk og design** Tore Eide, Inventas	**Scoreboarding** Espen Tallaksen, Bitvis
14:15	**Coffee break**	
Session 8	**Track AB: Closing Keynotes** Session chair: Hans Jørgen Fosse, Vitoteq	
14:45	**Closing Keynote: Edvard Sørgård, Graphics Architect, ARM Norway** ARM Mali graphics processors, the history and the technology	
15:30	**Closing Keynote: Erik N. Steen, Chief Engineer, GE Cardiovascular Ultrasound** Vivid E95 with cSound – A highly flexible system architecture	
16:15	Closing words	
~16:20	The end	

Keynotes:

- Opening keynote:
  Craig Davis, Senior Product Marketing Manager, Intel Programmable Solutions Group
  'Accelerating a Smart and Interconnected World'

- Closing keynote Day 1:
  Marius Fraurud, VP R&D, Tomra
  'The story of TOMRA. From a small Norwegian start-up to a large international company with a global footprint.'

- Closing keynote Day 2:
  Edvard Sørgård, Graphics Architect, ARM Norway
  ' *ARM Mali graphics processors, the history and the technology*'

- Closing keynote Day 2:
  Erik N. Steen, Chief Engineer, GE Cardiovascular Ultrasound
  'Vivid E95 with cSound – A highly flexible system architecture'

Price award for Best FPGA related Master thesis in Norway:

FPGA-Forum's price is given to the best FPGA related Master thesis in Norway.

The award committee:

- Dag Andreas Hals Samuelsen, University College of Southeast Norway (USN)
- Jim Tørresen, University of Oslo
- Hans Jørgen Fosse, Vitoteq

The nominees in alphabetical order:

- Ola Slettevoll Grøttvik, Dpt. of Physics and Technology, University of Bergen
  Supervisors: Kjetil Ullaland and Johan Alme
  'Design of High-Speed Digital Readout System for Use in Proton Computed Tomography'
- Lars Erik Songe Paulsen, Inst. for elektroniske system, NTNU
  Supervisors: Kjetil Svarstad and Milica Orlandic
  'Design and analysis of an H.265 entropy encoder'

All nominees will present their Master thesis in the last session (before closing keynote) on day 1. The winner will be announced during the dinner party.

One Workshop/Tutorial/Seminars Day 0, Tuesday 13th:

Deep Learning with MATLAB

Organiser: MathWorks

Location: Clarion Hotel & Congress Trondheim. **NOTE!**

Time: Tuesday, February 13: 14:00–16:00

Presenter: Daniel Aronsson

Cost: Free

Deep learning applications have rapidly evolved over the past decade and are now being used in fields varying from autonomous systems to medical image processing. This seminar focuses on deep learning techniques to help solve problems such as image classification. We will demonstrate how you can train a deep network and then use it, and we will examine ways to better understand how a deep network works. We will also show how a new tool, GPU Coder, makes it easy to deploy deep learning algorithms to desktop and embedded GPUs.

Link to registration and more info: https://se.mathworks.com/company/events/seminars/deep-learning-with-matlab-2346901.html?s_eid=PEP_16741

List of exhibitors (for Wednesday and Thursday):

- 4Test www.4test.no
- Arrow Norway (Intel FPGA) www.arrowne.com
- Avnet Silica (Xilinx) www.silica.no
- Bitvis www.bitvis.no
- Embida www.embida.no
- FirstEDA (Aldec) www.firsteda.com
- Innofour (Mentor) www.innofour.com
- MathWorks www.mathworks.com
- Microsemi (previously Actel) www.microsemi.com
- Synective Labs www.synective.se

Entertainment (during the dinner party):

Candiss

FPGA-forum Program-committee:

- Arild Kjerstad, Kongsberg
- Hans Jørgen Fosse, Vitoteq
- Jan Anders Mathisen, Silica/Xilinx
- Jim Tørresen, University of Oslo
- Per Gunnar Kjeldsberg, NTNU
- Espen Tallaksen, Bitvis

Titles and Abstracts for presentations at FPGA-forum 2018

(In company alphabetical order)

Note that written and oral presentations may be in English or Norwegian. Some presenters may also switch to English on Request
Presentations are thus marked 'Written' or 'Oral' and E (English), N (Norwegian) or EoR (English on Request)

Company & Presenter	**Title & Abstract**
4Test / Keysight Technologies Thomas Gøransson *Written: E, Oral: E*	**IOT from a power perspective** What are the challenges and what tools can be used and what are the limitations for different approaches. We will cover tools to generate and analyze power
Acando Robert Engels *Written: E, Oral: N*	**Hva er deep learning? Og hvorfor er FPGA relevant?** Hvordan henger kunstig intelligens, maskinlæring og deep learning sammen og hva er det egentlig? Hvilken rolle kunne FPGA spille i dette? Foredraget tar en gjennomgang gjennom temaene, viser hvordan deep learning fungerer og avslutter med betraktninger rund FPGAer, CPU/GPU og ASIC.
Alcatel Submarine Networks Norway Ole Henrik Waagaard *Written: N, Oral: N*	**Erfaringer med Vivado HLS for design av FPGA signalprosesseringskjede - C-design og testbenker** I Vivado HLS kompileres designet til VHDL/Verilog fra C/C++/SystemC- koden med direktiver som blant annet beskriver hvordan den sekvensielle C-koden skal parallelliseres i RTL-designet. For at HLS-kompilatoren skal kunne lage et gode VHDL-design bør man tenke dataflyt i C- designet og skrive C-strukturer som enkle og gjenkjennelige for kompilatoren. Noen retningslinjer for dette vil bli gitt. Det vil bli beskrevet hvordan ytelse og størrelse på designet kan endres ved hjelp av noen få direktiver uten å endre C-koden. Det vil også bli diskutert hvorfor man bør gå for et design i C++ og ta i bruk C++-templates. Testbenkene er skrevet i C/C++, og gir mulighet for å bruke allslags C- bibliotek i testbenken. Dette muliggjør test-drevet designmetodikk utviklet for C/C++.

Aldec Sergei Zaychenko *Written: E, Oral: E*	**Dealing with CDC verification complexity in large-scale FPGA designs** The number of interacting asynchronous clock domains has grown significantly over the last years in FPGA projects. Achieving CDC sign-off is equally important in today's FPGA designs as functional correctness, timing closure, power reduction, reaching optimal resource utilization. The existing dominating CDC verification methods and tools were designed mainly for the ASIC flow, and must be modified to be efficient in the context of FPGA. So what exactly is expected to be provided by a CDC tool for FPGA market? First of all, a correct interpretation of the built-in primitive libraries is a must, especially the clocking resources, memories, and serial I/O blocks. Most often, the provided simulation models aren't useful for CDC analysis, and cannot be synthesized directly. Some of the cells, however, have very complex timing expectations with multiple clocking and resetting modes, heavily dependent on generics. Second, the issues at the boundary with the IP blocks, mostly available in the encrypted form only without the detailed timing constraints. Then come the really advanced issues involving multiple dynamically switchable clock modes, exclusive clock groups, and reconfigurable design partitions, which dramatically increase the complexity of CDC verification. Manually describing all the tiniest timing properties of each cell in each mode is way too error-prone, and the tools must help with that. Another obstacle to deal with during the CDC sign-off is associated with preparing the correct timing constraints, as well as CDC-specific placement hints. A good CDC tool can help to generate the initial draft based on the topology, as well as check the existing constraints set for consistency and completeness. One of the biggest challenges is achieving the portability between vendor-specific SDC extensions. Finally, it is expected to have a straightforward interoperability between the tools for synthesis & implementation, CDC design rule checks, and functional CDC-aware simulation.
Altera	See Arrow
ARM Norway Edvard Sørgård *Written: E, Oral: E*	***** Closing Keynote, Day 2 ***** **ARM Mali graphics processors, the history and the technology** Edvard Sørgård is Director, GPU Hardware Engineering at Arm and has been working on the Mali graphics processors since its start-up origin in Falanx Microsystems in Trondheim, through the acquisition by Arm and the present day where they power much of today's mobile phones, tablets and digital TVs. Hear the story and get a view of the technology behind the Arm Mali graphics processors.
Arrow (Intel FPGA) Nikolay Rognlien *Written: E, Oral: EoR*	**Essential tools for FPGA board bring up.** As FPGAs have become the heart of an embedded system the tools needed to speedily bring a board up and allow easy debug have had to evolve. This presentation will highlight the tools and techniques available from Intel to help speed your through basic board bring-up and debug – getting your system out the door soonest!
Arrow (Intel FPGA) Nikolay Rognlien *Written: E, Oral: EoR*	**Accelerate FPGA development times with Intel's HLS compiler – a tutorial** Intel's new High Level Synthesis (or HLS) compiler allows customers to use C++ instead of the traditional Register Transfer Level (Verilog/VHDL) as the golden source for hardware design. In other words, using C++ instead of RTL raises the level of abstraction such that the model only needs to capture functional and high level architectural intent. This also allows users to execute the C++ program on a CPU, which enables them to verify code orders of magnitude faster than an event based RTL Simulator. Intel's HLS compiler understands C++ and performs various optimizations including generic compiler optimizations, FPGA-specific optimizations such as data path pipelining, and technology-specific optimizations (such as the ability to target hardened floating-point blocks on Stratix 10). The HLS compiler finally generates optimized production quality RTL code that can then be integrated into system designs with Qsys and then compiled with Quartus to generate the FPGA bitstream.
AvnetSilica (Xilinx) Jan Anders Mathisen *Written: E, Oral: N*	**FPGA-based compute acceleration – local systems and cloud based services** A look at current FPGA-based acceleration architectures, tools and services.

Bitvis Espen Tallaksen *Written: E, Oral: E*	**Scoreboarding** There is a lot of talk about scoreboards for FPGA (and ASIC) verification. This presentation will present some different angles on this subject and show how this can be done for relatively simple testbenches, and also for more advanced testbenches, all examples using straight forward VHDL and open source libraries. The planned ESA (European Space Agency) sponsored UVVM extensions will also be presented.
Cisco Systems Norway Jørgen Linnerud *Written: E, Oral: EoR*	**Python – What's the question?** Cisco utilize Python in build and tests systems, in-system debug and to auto-generate files in vhdl, system verilog, C, dts etc. The presentation will go through how Cisco at Lysaker uses Python in FPGA development.
FFI Sverre Brovoll *Written: N, Oral: N*	**FPGA in RIMFAX - a ground penetrating radar for NASA's Mars-2020 mission** RIMFAX is an instrument developed by FFI that is part of the instrument payload on NASA's Mars2020 rover that will be launched in 2020. RIMFAX will add a new dimension to the rover's toolset by providing the capability to image the subsurface structure beneath the rover. FPGA is a central component in the RIMFAX electronics design. This talk will give insight into the RIMFAX instrument, and the role of the FPGA in particular, and experiences and challenges met on the road from the radar lab to space.
GE Cardiovascular Ultrasound Erik N. Steen *Written: E, Oral: E*	***** Closing Keynote, Day 2 ***** **Vivid E95 with cSound – A highly flexible system architecture** – GEVU history/background – Quick introduction to cardiovascular ultrasound – Product introduction of Vivid E95 and overall architecture – The role of FPGAs in our system architecture (both passed and present) – Thoughts for the future
Hiddn Svein M Birkemoe *Written: E, Oral: EoR*	**Secure FW upgrade of embedded systems** Designing an embedded system handling confidential information and protecting the privacy of the user/owner is in itself challenging. In these days of IoT systems popping up all around us it is becoming more and more important that devices are protected from attacks. The encryption product explained in this session has implemented a safe method for FW updates which also enables an organization to control updates applied to their devices.
InnoFour (Mentor Graphics) Stefan Bauer *Written: E, Oral: E*	**Mastering Clock Domain Crossing challenges in FPGA Design** Metastabilty from the intermixing of multiple clock signals is not modeled by simulation. Unless you leverage exhaustive, automated Clock Domain Crossing (CDC) analyses to identify and correct problem areas, you will inevitably suffer unpredictable behavior when you go to the lab or when the FPGA is used in the field. Bottom-line: automated CDC verification solutions are mandatory for multi-clock designs. Designers increasingly use advanced multi-clocking architectures to meet the high-performance and low-power requirements of their chips. An RTL or gate-level simulation of a design that has multiple clock domains does not accurately capture the timing related to the transfer of data between clock domains. As a consequence, simulation does not accurately predict silicon behavior, and critical bugs may escape the verification process. The Questa CDC Solutions identify errors that have to do with clock domain crossings – signals (or groups of signals) that are generated in one clock domain and consumed in another. It does so with structural analysis and recognition of clock domains, synchronizers, and low power structures (via UPF); and with generation of metastability models for reconvergence verification. The technology checks all potential failure modes and presents to the user familiar schematic and waveform displays. Additionally, in concert with simulation this technology can be used to inject metastability into functional simulation to verify the DUT correctly processes asynchronous clocks.
Intel PSG / Intel FPGA	See Arrow

Intel FPGA Craig Davis *Written: E, Oral: E*	***** Opening Keynote ***** **Accelerating a Smart and Interconnected World** The world has entered the era of intellectualization and interconnection. The data center and cloud closely connect a vast array of devices, systems, and networks. With the deep deployment of Internet of Things (IoT), this fundamental transformation will affect not only single network connection nodes but also nearly all embedded and mobile electronic product systems. Therefore, many new diversified applications are born, and their development needs great programmatic flexibility, high performance, and high energy efficiency. Learn how Intel system design technology promotes the development of artificial intelligence, smart cities, industrial IoT and embedded vision and facilitates the building of the smart interconnected world.
Inventas Tore Eide *Written: N, Oral: N*	**Produktutvikling i grensesnittet elektronikk, mekanikk og design** Det forventes at produktene vi omgir oss med stadig blir smartere, og at de er sammenkoblet. Men hvordan kan vi utvikle gode produkter med robust mekanikk, lekkert design og smart elektronikk – og fortsatt ha brukerens behov i fokus?
Kongsberg John Aasen *Written: N, Oral: N*	**Godkjenning av missil med sikkerhetskritiske FPGAer** Kongsberggruppen har utviklet JSM, det eneste kryssermissilet som passer inn i bomberommet til F-35. Flere potensielt farlige funksjoner styres av FPGAer. Testing av missilet skjer i USA og krever at løsningene blir godkjent av Nonnuclear Munitions Safety Board. Dette er en lang prosess og erfaringene så langt presenteres.
MathWorks Daniel Aronsson *Written: E, Oral: E*	**Embedded GPUs: Compiling high-level vision and deep learning algorithms** There is an increasing interest in running deep learning and computer vision algorithms on embedded platforms, but it may be difficult to get adequate performance out of these embedded systems. One solution is to use platforms based on embedded GPUs, but such GPUs are difficult to program due to their parallel nature. With the advent of modern compilers that generate CUDA code from high level languages, we show how easy it has now become to deploy high-performance computer vision and deep learning applications on to embedded GPUs, including the Nvidia Jetson TX2 platform. We use a compiler to auto-generate portable and optimized CUDA code from a computer vision algorithm, which is then cross-compiled and deployed to the Tegra board. We will use examples of common computer vision algorithms and deep learning networks to describe this workflow, and we will present their performance benchmarks against commonly used deep learning frameworks.
Mentor Graphics	See Innofour
MicroSemi Anders Hillström *Written: E, Oral: E*	**Mi-V: a RISC-V based ecosystem – who needs another soft processor?** Unlike other processors RISC-V is a fixed instruction set that can be used for open source processor implementations. Since the instruction set is fixed and royalty free, software on a RISC-V processor implementation is easy to migrate between different implementations of the processor and different architectures like FPGA and ASIC. The open source code makes it easy to review the processor implementation in safety and security critical applications. Mi-V is Microsemi's implementation of a RISC-V based processor and a complete ecosystem with design tools, operating systems, solutions and evaluation boards.
NTNU Lars Lundheim *Written: N, Oral: N*	**Mellom vitskap og handverk - ingeniørutdanning for framtida.** Ingen veit eksakt korleis teknologien samfunnet vil sjå ut om 10 år. For best å møte dei utfordringane som kjem, treng me ei utdanning som gjev eit solid vitskapleg fundament, fremjar sjølvforståing og evne til samarbeid, og som dyrkar vilje og evne til å gå ut i ukjent terreng. Føredraget gjev døme på korleis me prøver nå desse måla i studieprogrammet Elsys: Elektronisk systemdesign og innovasjon.

PGS Geir Drange *Written: E, Oral: EoR*	**A low-power, full duplex, controlled spectrum modem link for single twisted pair power+communication applications** In some industrial applications there is a need to have both power and communications running on a single, unshielded twisted pair. There are multiple standards and commercial components that will do this, but none could satisfy all our requirements: No frequency content in the 1-500Hz range and otherwise a fully controlled spectrum, range > 200m, full duplex data rate > 30kbps, power < 50mW, cost < $15 and accurate (microseconds) real-time clock support. The solution was a modem design based on a very low power FPGA and only a few external components. Find out how the FPGA modem works and how pseudo random binary sequence generators are used to shape the link spectrum.
SINTEF Digital Dag K. W. Rognlien *Written: N, Oral: N*	**Erfaringer med Vivado HLS for design av FPGA signalprosesseringskjede - HLS fra en vhdl designers perspektiv** Erfaringer med HLS som design entry for FPGA – Vivado HLS gir deg mulighet til å bruke C/C++ som design entry. Dette gir mulighet til å beskrive noen konstruksjoner på en enklere måte og å samarbeide med andre som har C/C++ kunnskap om implementering. Det vil bli gitt noen eksempler på hva man tjener og hva man mister ved å bruke HLS, hva som genereres fra C/C++ koden og noen frustrasjoner over manglende detaljkontroll og tilsynelatende rare valg som HLS syntesen gjør.
Synective Labs Lars Forsberg *Written: E, Oral: E*	**FPGA in Neuroscience** In neuroimaging, the computational demand on the image processing pipelines is increasing as new methodological methods are improved. One computationally demanding method is to look at global brain connectivity in fMRI (functional MRI), where the brain activity of each voxel in the 3D brain volume is correlated over time with every other voxel to obtain a global measure of connectivity. Here, we look at how OpenCL on Intel Arria 10 FPGA can be used for parallel processing of fMRI data.
Thales Rune Bæverud *Written: E, Oral: N*	**Skyrocket FPGA team productivity with templates and standardized IP interfaces** Design high speed, low latency VHDL IP with focus on simplicity, quality, fast implementation and easy verification.
Tomra Marius Fraurud *Written: E, Oral: E*	***** Closing Keynote, Day 1 ***** **The story of TOMRA. From a small Norwegian start-up to a large international company with a global footprint** TOMRA was founded on an innovation for return of empty beverage containers more than forty years ago. In a small shed in Asker, Norway, the brothers Petter and Tore Planke created a solution to a problem: a local grocer wanted a machine that could quickly and easily take back empty bottles. This was the beginning of TOMRA. Today TOMRA is much more than just reverse vending machines. The company also brings its expertise in sensor-based technologies to other areas – like food sorting, municipal waste recycling, and mining. A spirit of entrepreneurship, a passion for innovation and a focus on finding solutions guide TOMRA to this day. From the world's first reverse vending machine in 1972, all the way to providing the most innovative sensor-based sorting solutions today, TOMRA has continuously redefined what it means to be innovative.
WideNorth Jean Bruant	**High-Speed Software Defined Radio -- Generic high-speed broadband SDR platform implemented in FPGA using direct sampling at L-band** Software-Defined Radios (SDRs) provides high flexibility both in term of design and use, and are already used in many satellite communication products. However, current SDR implementations typically support lower bandwidths and baud rates than what is required by new satcom applications operating in Ku-band, Ka-band, and Q/V-bands. Novel high-speed Analogue-to-Digital Converters (ADCs) and Digital-to-Analogue Converters (DACs) connected to new powerful FPGAs enable efficient SDR implementations of wideband satellite modems using direct sampling at IF. In this project we implemented a prototype for a wideband SDR platform for satellite communication supporting baudrates up to 400 Msps for QPSK and 8PSK modulation with direct sampling at L-band.
Xilinx	See Avnet Silica