FPGA
forum

FPGA-forum 2017

The 12th FPGA-forum – where the Norwegian FPGA community meets

- **FPGA-forum and exhibition: Wednesday 15 and Thursday 16 February 2017**
- **Tutorials/Workshops: Tuesday 14 February 2017**

At Royal Garden Hotel (Trondheim)

FPGA-forum er den årlige møteplassen for FPGA-miljøet i Norge. Her samles FPGA-designere, prosjektledere, tekniske ledere, forskere, siste års studenter og de største leverandørene på ett sted for 2 dagers praktisk fokus på FPGA.

Det blir foredrag fra norske bedrifter om utviklingsmetodikk og praktisk erfaring, universitetene presenterer nye og spennende prosjekter, og leverandørene stiller med aktuelle tekniske innlegg med et minimum av markedsføring. På utstillingen vil du kunne vurdere teknologi og verktøy fra de ledende leverandørene i bransjen.

FPGA-forum byr i tillegg på en ypperlig anledning til å møtes og utveksle erfaring innenfor FPGA-miljøet i Norge - både i pausene og under det sosiale arrangementet på kvelden.

In English:

FPGA-forum is a yearly event for the Norwegian FPGA community. FPGA-designers, project managers, technical managers, researchers, final year students and the major vendors gather for a two-day focus on FPGA.

There will be presentations from the Norwegian industry about methodology and practical experience, - the universities will present new and exciting projects, and the vendors will have technical presentations with a minimum of marketing. At the exhibition, you can evaluate tools and technology from the leading vendors.

FPGA-forum also provides an excellent opportunity to meet and exchange experience with the Norwegian FPGA-community – during the breaks – and during the official dinner party on Wednesday.

Programme Wednesday, February 15, 2017 (Note: See appendix for abstracts)

09.00	Registration and coffee	
Session 1	**Track AB**	
09.25	**Opening**	
09.30	**Keynote by Liam Madden,** **Corporate Vice President, FPGA Development and Silicon Technology, Xilinx** 'The rise of massively parallel processing: Why the demands of big data and power efficiency are changing the computing landscape'	
10.30	**Vendor presentations** (3 min. per exhibitor - in order as shown on page 4))	
11:10	**Coffee break (and exhibition)**	
Session 2	**Track A** Session chair: Jørgen Linnerud, Cisco	**Track B** Session chair: Sverre Vigander, Bitvis
11.40	**Linux device-tree, guds gave til software utviklere?** Tore Fleten, Cisco Systems Norway	**Partial reconfiguration – the underrated feature of FPGA technology** Jan Anders Mathisen, Avnet Silica (Xilinx)
12:10	**FINN: A Framework for Fast, Scalable Binarized Neural Network Inference** Magnus Jahre, NTNU	
12:40	**Lunch and Exhibition**	
Session 3	**Track A** Session chair: Arild Wego, Tomra	**Track B** Session chair: Knut Wold, NTNU
14:00	**FPGAs in Machine Learning applications** Nikolay Rognlien, Arrow (Altera)	**Intro to security in FPGAs** Arne Rogndalen, Data Respons
14:30	**Hardware Acceleration Platform on Altera Cyclone V SoC FPGA** Sigurd Øyen, Embida	**CAE Based Physics of Failure Analysis (PoF) Makes Design for Reliability (DfR) Integrated Part of PCB Design** Yehoshua Shoshan, InnoFour (DfR Solutions)
15:00	**Verifying the Numascale UPI node controller ASIC using Intel BFMs and Intel Skylake Cosimulations** Thomas Moen, Numascale	**How to burn up lots of energy on presumptously large amounts of FPGA silicon, and still be proud of it -- or, computing that which you don't know exactly how to compute.** Kjetil Svarstad, NTNU
15:30	**Exhibition and Coffee**	
Session 4	**Track A** Session chair: Hans Jørgen Fosse, Mikrokrets	**Track B** Session chair: Svein Haustveit, Western Norway University of Applied Sciences (HVL)
16:00	**Take control over your power consumption!** Thomas Gøransson , 4TEST/Keysight Technologies	**Continuous Integration for FPGA Development** Halvard Brennum, AppearTV
16:30		**Novice FPGA designers – A major risk in most projects** Espen Tallaksen, Bitvis
17:00	**End of today's presentations**	
19.00	Aperitif, Royal Garden Hotel	
19.30	Entertainment with a twist – never previously seen at FPGA-forum.	
20:00	Dinner party, Royal Garden Hotel.	

Programme Thursday, February 16, 2017 (Note: See appendix for abstracts)

Session 5	**Track A** Session chair: Jørgen Norendal, University of Oslo	**Track B** Session chair: Hans Jørgen Fosse, Mikrokrets
09.00	**Low power Imaging and Video solutions in Microsemi FPGAs** Anders Hillström , MicroSemi	**Prototyping the Numascale UPI node controller ASIC using Intel Xeon+FPGA and Altera FPGAs** Stein Kjølstad, Numascale
09:30	**Design Methodology for Rapid Prototyping and Early Verification in FPGA and SoC Design** Jonas Rutström, Mathworks	**Methodology for RTL development in Graphic** Carmelo Giliberto, ARM
10:00	**Automatic Formal Checks for FPGA designs** Rick Stroot, InnoFour (Mentor Graphics)	
10.30	**Exhibition and Coffee**	
Session 6	**Track A.** Session chair: Chato Jakobsen, Informasjonskontroll	**Track B** Session chair: Kjetil Svarstad, NTNU
11:00	**Register map fra FPGA, software utviklers mareritt!** Tore Fleten, Cisco Systems Norway	**Can Internet teaching replace lectures and labs?** Jim Tørresen and Jørgen Norendal, University of Oslo
11:30	**Auto generating code and generic FPGA register access from software** Michal Koziel, Bitvis	**Towards Ubiquitous Low-Power Image Processing Platforms (TULIPP)** Magnus Jahre, NTNU
12:00	**Lunch and Exhibition**	
Session 7	**Track A** Session chair: Carmelo Giliberto, ARM	**Track B** Session chair: Magnus Jahre, NTNU
13:15	**Software enabled threaded programming of FPGAs using Partial Reconfiguration** Dirk van den Heuvel, Topic Products	**Stratix 10 MX, Bandwidth challenge solved with integrated DRAM** Jonas Åström, Arrow (Altera)
13:45	**Erfaringer med bruk av partiell rekonfigurering i Xilinx FPGA** Simen Gimle Hansen, Kongsberg Defence Systems / Defence Communications	**Challenges with using FPGA for Functional Safety** Dag Kristian Rognlien, Sintef
14:15	**Coffee break**	
Session 8	**Track AB: Closing Keynotes** Session chair: Per Gunnar Kjeldsberg, NTNU	
14:45	**Closing Keynote: Haakon Bryhni, Chief Technology Officer, Elliptic Labs** Development of a software-based ultrasound sensor technology for the smartphone market, from IP to OEM integration and market introduction in Asia.	
15:30	**Closing Keynote: Gaute Myklebust, CTO, MyWo AS and Vegard Wollan, CEO, MyWo AS** The Atmel story – 20 years with innovation as the key success criteria	
16:15	Closing words	
16:20	The end	

Keynotes:

- Opening keynote:
  Liam Madden, Corporate Vice President, FPGA Development and Silicon Technology, Xilinx
  'The rise of massively parallel processing: Why the demands of big data and power efficiency are changing the computing landscape'
- Closing keynote Day 2:
  Gaute Myklebust: CTO, MyWo AS and
  Vegard Wollan: CEO, MyWo AS
  '*The Atmel story – 20 years with innovation as the key success criteria*'
- Closing keynote Day 2:
  Haakon Bryhni, Chief Technology Officer, Elliptic Labs
  'Development of a software-based ultrasound sensor technology for the smartphone market, from IP to OEM integration and market introduction in Asia'

List of exhibitors (for Wedn. 15th and Thur. 16th):

- 4TEST/Keysight Technologies www.4test.no
- Arrow Norway (Altera) www.arrowne.com
- Avnet Silica (Xilinx) www.silica.no
- Bitvis www.bitvis.no
- Doulos www.doulos.com
- Embida www.embida.no
- Innofour (Mentor) www.innofour.com
- MathWorks www.mathworks.com
- Microsemi (previously Actel) www.microsemi.com
- ProgBit www.progbit.no
- Synective www.synective.se
- Topic Products www.topicproducts.com

Entertainment (during the dinner party):

Surprise ☺

Two Workshops/Tutorials Day 0, Tuesday 14th:

Please note that the tutorials run in parallel.

Workshop A:

FPGA and SoC Design using MATLAB and Simulink

Organiser: Mathworks

Link to registration and more info: https://go2.mathworks.com/fpga-workshop-sem-se-1857105

Please note:
The Workshop is free of charge.
You need to bring your own laptop to the Workshop.
This workshop is not open for students.

Workshop B:

Introduction to OpenCL SDK for Intel FPGA

Organiser: Arrow Norway

Description: In this workshop, we will first give an overview the High Level Design (HLD) tools for Intel FPGAs and then look more closely into the OpenCL SDK.
During the hands-on session, the participants will use the OpenCL for FPGA compiler on a few examples, learn to interpret the information given in the optimization and area reports and learn to improve the examples.

Presenters:
Suleyman Demirsoy, DSP Technology Specialist at Intel (+Nikolay Rognlien, Arrow)

Prerequisites:
Bring your own laptop with VMware Workstation Player(version 12) installed.
http://www.vmware.com/products/player/playerpro-evaluation.html
You will be given a Virtual Machine with all necessary software preinstalled when attending the workshop.

Time and place:
Tuesday February 14th, 10:00 to 15:00
Radisson Blu Royal Garden Hotel, Trondheim

Please note
The Workshop is free of charge, but limited seating.
Registration to: pkristiansen@arroweurope.com

FPGA-forum Program-committee:

- Arild Kjerstad, Kongsberg
- Hans Jørgen Fosse, Mikrokrets
- Jan Anders Mathisen, Silica/Xilinx
- Jim Tørresen, University of Oslo
- Per Gunnar Kjeldsberg, NTNU
- Espen Tallaksen, Bitvis

Titles and Abstracts for presentations at FPGA-forum 2017

(In company/university alphabetical order)

Note that written and oral presentations may be in English or Norwegian. Some presenters may also switch to English on Request
Presentations are thus marked 'Written' or 'Oral' and E (English), N (Norwegian) or EoR (English on Request)

Company & Presenter	Title & Abstract
4TEST/Keysight Technologies Thomas Gøransson *Written: E, Oral: E*	**Take control over your power consumption!** The goals for this presentation is to make you feel a little bit more confident about the power integrity measurements that you make and show you some tips, techniques, tools, so you can make more accurate and precise measurements then you'll be better armed to more quickly isolate your root problems in your design. There's this sudden emergence and urgency with people to make better power integrity measurements. It is the increased functional density of all the hand-held products and industrial products and medical products and internet of things and computing products has driven power density problems, and that has caused designers to result to tighter supply tolerances and reducing supplies. Maybe even the biggest issue that everybody's running into is the notion of power supply induced jitter. Power supply noise can be the biggest single cause of clock and data jitter in their systems. Different tools for power measurement will be presented.
Aldec	See FirstEDA
Altera	See Arrow
AppearTV Halvard Brennum *Written: E, Oral: EoR*	**Continuous Integration for FPGA Development** Continuous Integration (CI) tools have been commonly used in software development for years. All committed code is built automatically, and regression tests are performed regularly. At Appear TV we have seen the advantages of CI in SW development, and applied this to our FPGA development flow. We will present our experience from automating VHDL compilation, VHDL simulation, FPGA build and FPGA regression test. We will also give a short introduction to our CI-tool Jenkins.
ARM Carmelo Giliberto *Written: E, Oral: E*	**Methodology for RTL development in Graphic** GPUs were initially designed to accelerate computation for computer graphics, however they have developed to a level where they can be used many real world applications such as computer vision, virtual and augmented reality, machine learning and robotics. HW design of these units has become extremely complex. Engineers are often challenged to design smaller, faster and more energy efficient HW. At the same time the feature-set is constantly increasing and the time-to-market reduced. RTL development methodology is a key factor in facing these challenges. This presentation gives an overview of the design and test methodology we have developed in ARM. The methodology includes flows for ensuring functional correctness and efficient diagnosis and debugging of failures, as well as flows for measuring and tracking performance, area, clock frequency, energy and power. Clever architectural innovations paired with our highly efficient design and test flows, enabled the team to increase the performance per area for a particular block by a factor of 2 in a single year.

Arrow (Altera) Nikolay Rognlien *Written: E, Oral: EoR*	**FPGAs in Machine Learning applications** Machine learning is one of the fastest growing application models, and crosses every vertical market from the data center, to embedded vision applications in the IoT space, to medical and industrial applications. This presentation introduces the high-level concept of machine learning, focusing on Convolutional Neural Networks. It also explains the benefits of using an FPGA in these applications.
Arrow (Altera) Jonas Åström *Written: E, Oral: E*	**Stratix 10 MX, Bandwidth challenge solved with integrated DRAM** Memory bandwidth is a critical bottleneck for next-generation platforms. The critical path in any system's performance is the system's ability to process large amounts of data quickly. To meet exploding memory bandwidth requirements, system designers have attempted to use currently available conventional technologies. However, these conventional technologies pose a number of challenges. Join this session to learn how the new Stratix10 MX help overcome these challenges by integrating large amounts of DRAM together with the FPGA.
Avnet Silica (Xilinx) Jan Anders Mathisen *Written: E, Oral: EoR*	**Partial reconfiguration – the underrated feature of FPGA technology** Partial reconfiguration (PR) is a term describing the ability to reconfigure parts of an FPGA while the rest of the device operates undisturbed. Xilinx has offered devices with various levels of PR capabilities for more than 20 years and the feature has been the theme of several previous presentations at FPGA-Forum. Although a powerful and intriguing feature – PR has yet to become a mainstream part of the FPGA designer's toolbox. The presentation looks at the current state of Xilinx PR core device technology and tools and intends to encourage the audience to take PR into consideration when planning their next design.
Bitvis Michal Koziel *Written: E, Oral: N*	**Auto generating code and generic FPGA register access from software** Software and FPGA developers often struggle with synchronization of the register map. Parallel register access from multiple software applications is also a difficult issue to deal with. Auto generation of code from a single source keeps the register map synchronized. Centralized register access in software solves many problems related to parallel register access.
Bitvis Espen Tallaksen *Written: E, Oral: E*	**Novice FPGA designers – A major risk in most projects** Unfortunately, novice FPGA designers have not even close to sufficient knowledge on proper FPGA development. Many companies can seemingly live with the fact that this results in a significantly longer development time, but do they really know the risk they are taking with respect to quality? Bad design often leads to bugs that are really hard to detect even in the best lab and system tests, - but they will show up sooner or later. One might of course argue that experience is something you gain once you start working, and that is true, - but this is not about lack of experience; - This is about lack of very important basic knowledge. Strangely enough there seems to be very little focus on this - even in the larger companies. Yes, they do have reviews, and yes, they do give feedback, - and that is good, - but not at all sufficient. This of course also means that the default learning curve is really slow, - and hence the problem does not only apply to novice FPGA designers… This presentation will give a very brief introduction to the subject and then show how we approach this challenge in Bitvis.
Cisco Systems Norway Tore Fleten *Written: E, Oral: N*	**Linux device-tree, guds gave til software utviklere?** Device-tree (dts) blir brukt mer og mer til å konfigurere lasting av Linux drivere. Vil gå igjennom historien bak dts, og bruk av dts for drivere som kjører mot/på FPGA.
Cisco Systems Norway Tore Fleten *Written: E, Oral: N*	**Register map fra FPGA, software utviklers mareritt!** Blir stadig større utfordring å holde FPGA, register map og drivere/software i synk. Vil gå igjennom hvordan man i software kan få konfidens, at FPGA og register map hører i sammen, fra Linux programmer til Linux kernel drivere.

Data Respons Arne Rogndalen *Written: E, Oral: N*	**Intro to security in FPGAs** How to leverage FPGAs in secure systems. Types of FPGAs, design methodology including Isolation Design Flow, cryptographic primitives, and secure design practices against attacks.
Elliptic Labs Haakon Bryhni *Written: E, Oral: E*	***** Closing Keynote, Day 2 ***** **Development of a software-based ultrasound sensor technology for the smartphone market, from IP to OEM integration and market introduction in Asia** The presentation will explain launch of a novel signal processing technology for proximity sensing and gesture recognition which has been successfully implemented in one of the large Chinese mobile OEMs (see for example http://www.theverge.com/2016/10/25/13401600/xiaomi-mi-mix-iphone-8-preview). A key to this success is the ability to realize a proximity sensor behind glass, and to leverage the powerful DSP processing infrastructure in a modern smartphone. Another essential factor is the process of gaining access to the Asian market. The presentation will touch on both, as well as future use of the technology for a wide range of natural, touch-less gestures, evolving the standard user interface for smartphones.
Embida Sigurd Øyen *Written: E, Oral: N*	**Hardware Acceleration Platform on Altera Cyclone V SoC FPGA** This is a school project exploring opportunities of lowering the threshold for utilizing hardware acceleration. The project is about development of a software oriented platform for hardware acceleration. It is implemented in an Altera Cyclone V SoC FPGA and controlled from software using Python.
InnoFour (Mentor Graphics) Rick Stroot *Written: E, Oral: E*	**Automatic Formal Checks for FPGA designs** RTL designers can't wait for a test bench to begin checking the quality of their code and verifying the functionality they've started to implement is on the right track. Assertion-based verification can be employed, but even basic properties in standard languages like SVA or PSL are time consuming to create, debug, and maintain. The Questa AutoCheck app makes it easy to triage bugs that would otherwise require a lot of time and effort to eliminate, such as state-machine deadlock and livelock, arithmetic overflow, out-of-range memory indexing and many more. AutoCheck's rich debugging environment pinpoints the root cause of these bugs with schematics, waveforms and FSM state diagrams, making it quick and easy to use.
InnoFour (DfR Solutions) Yehoshua Shoshan *Written: E, Oral: E*	**CAE Based Physics of Failure Analysis (PoF) Makes Design for Reliability (DfR) Integrated Part of PCB Design** Computer Aided Engineering software enables usage of reliability calculation based on physics of failure methodology. In this presentation we will give an overview of PoF, the justification to use it, how it stands in comparison to other methodologies and how it is implemented in CAE software. Finally we will also explain the impact of PoF on a design.
Kongsberg Defence Systems / Defence Communications Simen Gimle Hansen *Written: E, Oral: N*	**Erfaringer med bruk av partiell rekonfigurering i Xilinx FPGA** Kongsberg Defence & Aerospace avd. kommunikasjon har i forbindelse med utviklingen av RL542A Radiolinje for Bånd 4 valgt å ta i bruk partiell rekonfigurering av Xilinx FPGA. Partiell rekonfigurering er implementert i MIPU (Modem and Interface Processing Unit) FPGAen i RL542A. MIPU FPGAen utfører all signalprosessering i RL542A og er implementert i en Xilinx Kintex-7 XC7K325T FPGA. Det er per i dag implementert to forskjellige multirate modem i MIPU. Et fast frekvens m-QAM (4-, 16-, 64-QAM; 512K, 1M, 2M, 4M, 8M, 16M, 34M, 70M, 100Mbit/s) modem og et frekvens hoppende m-PSK (2-, 4-, 8-PSK; 512K, 1M, 2M, 4M, 8Mbit/s) modem. Modemene er implementert med MathLab, Simulink og HDL Coder. De andre modulene i kretsen er implementert i VHDL. Det er modemet i MIPU FPGAen som er partielt rekonfigurerbar. Vi har brukt Vivado sin Partial Reconfiguration Design Flow i non-project mode til å implementere partiell rekonfigurering i MIPU. Vi vil i denne presentasjonen presentere våre erfaringer med bruk av partiell rekonfigurering i utviklingen av RL542A.

Mathworks Jonas Rutström *Written: E, Oral: E*	**Design Methodology for Rapid Prototyping and Early Verification in FPGA and SoC Design** High-level programming languages are frequently used by FPGA engineers to accelerate product design. In this presentation, we will use our industry knowledge to summarize the best programming practices adopted by FPGA designers to enable early verification and rapid prototyping of hardware algorithms. This will help you minimize the number of bugs found late in the design process where the cost of correction is painfully high compared to dealing with them at an early stage. We hope to inspire you to investigate new powerful solutions that take you and your colleagues into the next level of product development. • Design higher and increase your flexibility • Use simulation to gain confidence in your design • Maximize your productivity with automated verification and implementation of FPGA and SoC designs • Partitioning of HW/SW systems using MATLAB/Simulink • From idea to product – different phases different tools!
Mentor Graphics	See Innofour
MicroSemi Anders Hillström *Written: E, Oral: E*	**Low power Imaging and Video solutions in Microsemi FPGAs** The adaptable nature of FPGAs is well suited for video applications in different imaging systems. Image sensors use a number of different interfaces and need to be configured in different ways. Low heat dissipation is key to low noise in the captured image. Flash based FPGAs provide a low power platform for the image sensor interface, video signal processing, video compression and display interface. A wide range of free basic imaging/video IPs from Microsemi together with 3rd party IPs reduces the design effort and shortens development time.
MyWo Gaute Myklebust and Vegard Wollan *Written: E, Oral: E*	***** Closing Keynote, Day 2 ***** **The Atmel story – 20 years with innovation as the key success criteria** Gaute Myklebust and Vegard Wollan were co-founders of Atmel Norway in 1995. They met each-other at NTH (NTNU) where the AVR was invented. In over 20 years they have been key players in the leadership team of the continuously growing microcontroller business of Atmel Corp. Gaute and Vegard will share with FPGA forum some of the key success criteria behind the Atmel and AVR story.
NTNU Magnus Jahre *Written: E, Oral: EoR*	**Towards Ubiquitous Low-Power Image Processing Platforms (TULIPP)** Industrial vision-based applications with stringent performance, power and cost requirements are becoming ubiquitous. Unfortunately, the development of such systems is a labor-intensive and challenging process. The problem is exacerbated by the lack of standards which result in substantial overhead when moving a system from one platform to another. The TULIPP Horizon 2020 EU-project will work towards reducing the impact of these problems by defining a reference platform for high-performance, low power, embedded image processing that can contribute to accelerating standardization processes. The reference platform is presented in the context of the starter kit, a conceptual package consisting of the platform instance, project applications and reference platform handbook. The aim of the starter kit is to provide engineers with a generic evaluation platform that serves as a base for productively developing low power image processing applications. The starter kit is validated using key applications from the medical, UAV and automotive domains.
NTNU Kjetil Svarstad *Written: E, Oral: EoR*	**How to burn up lots of energy on presumptously large amounts of FPGA silicon, and still be proud of it -- or, computing that which you don't know exactly how to compute.** Non-determinism is a powerful concept, useful in everything computer theoretical from algorithmic complexity to the definition and underlying semantics of regular languages and grammars. Also, it can be mapped into a large set of diverse automatons useful in analysis and verification of both hardware and software. However, we are interested in using non-deterministic automata and state machines to execute an incomplete specification of a computational problem. We have thus defined a non-deterministic execution principle that utilises self-reconfiguration of FPGAs, and that allows the computation of non-restricted, underspecified and possibly conflicting alternative futures with a causal purging of alternatives whenever an event establishes a strictness in a future become actual. We will present the downsides and upsides of this principle, show how we have implemented it, and hopefully say something about for what is can be useful... and how fun it is!

NTNU Magnus Jahre *Written: E, Oral: E*	**FINN: A Framework for Fast, Scalable Binarized Neural Network Inference** Research has shown that convolutional neural networks contain significant redundancy, and high classification accuracy can be obtained even when weights and activations are reduced from floating point to binary values. These Binarized Neural Networks (BNNs) are particularly well suited to reconfigurable logic devices, which contain an abundance of fine-grained compute resources and can result in smaller, lower power implementations, or conversely in higher classification rates. This talk will present FINN, a framework for building fast and flexible FPGA accelerators for BNNs using a flexible heterogeneous streaming architecture. FINN-generated accelerators can perform accurate image classification at unprecedented speeds. Key results include classification of handwritten digits with 95.8% accuracy at 12.3 million frames per second and classification of CIFAR-10 images with 80.1% accuracy at 22 thousand frames per second, both on an embedded FPGA platform drawing less than 25 W total system power.
Numascale, Thomas Moen *Written: E, Oral: EoR?*	**Verifying the Numascale UPI node controller ASIC using Intel BFMs and Intel Skylake Cosimulations** Numascale combines their knowledge of doing node controllers with state of the art Intel Xeon CPUs to build some of the most powerful shared memory systems. The Intel UltraPath Interconnect, UPI, is a point-to-point processor interface. Numascale's node controller hook onto UPI and provides a high performing, cache coherent connection between 32 CPU sockets, or beyond. Design verification of such a complex chip is challenging. Numascale uses a combination of BFM driven RTL simulations and Intel Skylake RTL cosimulations to push for first-time-right on the ASIC. Key design criteria are low latency and high bandwidth. Bidirectional bandwidth to local CPUs is 75 GB/s and aggregated bandwidth to external nodes is 200 GB/s. Numascale will share a description of the chip and their experience and plans on doing BFM driven simulations and working with Intel on simulating the node controller with real Skylake RTL.
Numascale, Stein Kjølstad *Written: E, Oral: ?*	**Prototyping the Numascale UPI node controller ASIC using Intel Xeon+FPGA and Altera FPGAs** Numascale combines their knowledge of doing node controllers with state of the art Intel Xeon CPUs to build some of the most powerful shared memory systems. The Intel UltraPath Interconnect, UPI, is a point-to-point processor interface. Numascale's node controller hook onto UPI and provides a high performing, cache coherent connection between 32 CPU sockets, or beyond. Design verification of such a complex chip is challenging. Numascale uses FPGA prototyping to support simulations and push for first-time-right on the ASIC. Numascale will share their experience and plans for the FPGA prototype. The FPGA prototype will consist of eight Intel Neon-City servers, each holding two Xeon+FPGA processors, using Arria10 FPGAs. Eight multi-purpose FPGA boards holding two StratixV size AB FPGAs and DDR memories will be used to emulate the core functions of the node controller.
Sintef Dag Kristian Rognlien *Written: E, Oral: N*	**Challenges with using FPGA for Functional Safety** Embedded platforms serving safety critical systems must adhere to strict requirements regarding functional safety as defined in e.g. IEC 61508 or similar domain specific standards. Developing hardware and software according to such standards is often more complex, expensive and time consuming than "traditional" development due to requirements regarding documentation, traceability, methodology and lifecycle management. The safety standards mostly do not directly address the specific issues of the FPGA technology. From a safety standard perspective development for FPGA may be considered as an hybrid between hardware and software, but has traditionally been certified according to hardware requirements. In this talk we will address some of the challenges when integrating complex FPGA designs in safety critical embedded systems.

Topic Products Dirk van den Heuvel *Written: E, Oral: E*	**Software enabled threaded programming of FPGAs using Partial Reconfiguration** As FPGAs become larger and larger, the amount of functionality that fit in an FPGA increases in a similar pace. To be able to fill this functionality you need higher productivity or more FPGA engineers. To address both aspects, you need to improve productivity as well as the potential number of engineers. The closely coupled integration capabilities of the current generation of System-on-Chips require software- and FPGA developments to be mixed together very intimately. It is interesting to see that, where software designers nearly always deploy an operating system on their processor, FPGA designers start often from scratch. Re-use strategies are becoming more common, but operating system style infrastructures of FPGAs are rarely in place or publicly available. However, using Partial Reconfiguration of FPGA fabric in combination with a well-integrated infrastructure on the FPGA allow a form of threaded FPGA use, just like software. When exploring this technology further on the FPGA and projecting this on fail-safe and fault-tolerant computing and even on single event upset mitigation, Partial Reconfiguration can be considered as an under estimated technology. In this presentation, Partial Reconfiguration technology will be discussed in terms of use cases and principle functioning. The exploit of PR will be illustrated using a few examples and discussing implementation considerations, such as an operating system on FPGA fabric. The actual usage will be demonstrated live to show in what way it can be applied and how even software developers can benefit to deploy their functionality on the FPGA with little involvement of an FPGA designer.
UiO Jim Tørresen and Jørgen Norendal *Written: E, Oral: EoR*	**Can Internet teaching replace lectures and labs?** To reduce the challenge of learning reconfigurable hardware design, we have developed a framework for flexible learning through Internet. Learning takes place using videos, lecture slides, quizzes and lab assignments in addition to regular text books. Lab assignments consist of a physical lab setup accessible through a web browser. In this talk, we present the developed material and student feedback after using it.
Xilinx Liam Madden *Written: E, Oral: E*	***** Opening Keynote ***** **The rise of massively parallel processing: Why the demands of big data and power efficiency are changing the computing landscape** We live in a world where we generate more data than we can reasonably digest, communicate and entertain ourselves using streaming video and look forward to a future where every sensor in our environment will be instantly available in the cloud. Each of these trends puts huge demands on both communication and compute performance but with no commensurate increase in cost, power or thermal budgets. In the past 15 years we have seen a move from single core, mainly serial computation, to parallel heterogeneous systems. In this talk we will explore the motivations for this shift in architecture and speculate on what the future may hold
Xilinx	See also Avnet Silica