Tekna

FPGA forum

The 8th FPGA-forum – where the Norwegian FPGA community meets

FPGA-forum and exhibition: Wednesday 13. and Thursday 14. February 2013

Britannia Hotel (Trondheim)

FPGA-forum is a yearly event for the Norwegian FPGA community.
FPGA-designers, project managers, technical managers, researchers, final year students and the major vendors gather for a two-day focus on FPGA.

There will be presentations from the Norwegian industry about methodology and practical experience, - the universities will present new and exciting projects, and the vendors will have technical presentations with a minimum of marketing. At the exhibition you can evaluate tools and technology from the leading vendors.

FPGA-forum also provides an excellent opportunity to meet and exchange experience with the Norwegian FPGA-community – in the breaks – and during the official dinner party on Wednesday.

Program Wednesday, February 13, 2013 (Note: See appendix for abstracts)

09.00	Registration and coffee	
Session 1	**Track AB** Session chair: Espen Tallaksen, Bitvis	
09.25	**Opening**	
09.30	**Keynote by Dennis Segers, CEO, Tabula Inc.** Programmable logic technology; Enabling a "Renaissance of Innovation"	
10.30	**Vendor presentations** (3 min. per exhibitor - in alphabetical order)	
11:10	**In memory of Einar Johan Aas – a nestor in the Norwegian electronics design community.** Kjetil Svarstad	
11:25	**Coffee break (and exhibition)**	
Session 2	**Track A** Session chair: Håvard P Alstad, Data respons	**Track B** Session chair: Jim Tørresen, UiO
11.45	**System verifikasjon av FPGA IO** Tore Fleten, Cisco	**What FPGA designers can learn from the software guys** Philippe Faes, Sigasi
12.15	**Xilinx - Enabling New Product Innovations Across Markets with Zynq SoC and Vivado HLS** Olivier Tremois, Xilinx	**Smartfusion2 SoC FPGA** Peter Trott, MicroSemi
12:45		**Assertion Based Verification in Dynamic Reconfigurable Systems Using Functional Abstractions** Bahram Najafi-Uchevler, NTNU
13.15	**Lunch and exhibition**	
Session 3	**Track A** Session chair: Arild Kjerstad, Kongsberg	**Track B** Session chair: Hans Jørgen Fosse, Mikrokrets
14:30	**SystemVerilog for Configurable Designs** Odd Magne Reitan, Atmel	**FPGA SoCs – A Centerpiece for Digital Design** Antti Innamaa, Synopsys
15:00		**The impact of requirement traceability in safety critical designs** Rick Stroot, InnoFour (Mentor Graphics)
15:30	**Altera versus Xilinx** Dagrun Røyrvik, Cisco	**An efficient hardware architecture design for H.264/AVC intra prediction reconstruction path using dynamic partial reconfiguration** Milica Orlandić, NTNU
16.00	**Coffee break (and exhibition)**	
Session 4	**Track A** Session chair: Hans Jørgen Fosse, Mikrokrets	**Track B** **Session chair:** Arild Kjerstad, Kongsberg
16.30	**Presentation of the 3 Master's theses nominated for the FPGA-forum award** *(see page 4)* *(Note: The award is given during the dinner party)*	**Erfaringer med System Verilog/UVM testbenker** Ove Brynestad, Cisco
17:00		**Design reuse of both HW and SW – The topic of verifying and designing hetrogenious systems with ARM CPUs and High level design Synthesis.** Tryggve Mathiesen, Informasic
17.30	**End of today's presentations**	
19.30	Aperitif in the 'Lobby Lounge' outside 'Speilsalen', Britannia Hotel	
20.00	Dinner party in the 'Speilsalen', Britannia Hotell. - Entertainment: Studentkoret Candiss	

Program Thursday, February 14, 2013 (Note: See appendix for abstracts)

Session 5	**Track A** Session chair: Tryggve Mathiesen, Informasic	**Track B** Session chair: Bjørn B Larsen, NTNU
09.00	**QSys - Conquer FPGA Design Complexity with System-Level Integration** Amar Abid-Ali, EBV	**FPGA i satellitt, demodulasjon i Command Receiver** Espen Flo Eriksen, Kongsberg Norspace
09.30	**Providing Linux tool chains, kernel and build system for SoC based FPGAs** Hans Christian Lønstad, Data Respons	**OS-VVM: High-Level VHDL Verification** Ian Gibbins, FirstEDA (Aldec)
10.00	**FPGA with ARM processor system on-chip…** Nikolay Rognlien, Arrow (Altera)	
10.30	**Coffee break (and exhibition)**	
Session 6	**Track A.** Session chair: Tryggve Mathiesen, Informasic	**Track B** Session chair: Atle Tangedal, Tekna
11.15	**Understanding legacy code** Philippe Faes, Sigasi	**Effektiv bruk av eksternt minne** Håvard Pedersen Alstad, Data Respons
11.45	**User experience designing a FPGA for transfer 5.5 GByte/s from an analog frontend, into a pc for digital processing.** Morten Haugen, GE Vingmed/Healthcare	**Key Challenges in the analysis and design of high speed digital links** Thomas Göransson, Agilent (4Test Instruments)
12.15	**Achieving the right FPGA design quality – Could reviews save the day?** Espen Tallaksen, Bitvis	
12.45	**Lunch and Exhibition**	
Session 7	**Track A** Session chair: Jim Tørresen, UiO	**Track B** Session chair: Fredrik Stray, Bitvis
14.15	**Designing and constraining Clock Domain Crossings** John Aasen, Kongsberg	**Implementing DSP Algorithms on FPGAs using MATLAB and Simulink** Jonas Rutström, Mathworks
14.45	**Integration and Verification of Multiple-clock Domain FPGA Designs** Reuven Dobkin, vSync Circuits	**Open CL in fpga** Nikolay Rognlien, Arrow (Altera)
15.15	**Coffee break**	
Session 8	**Track AB** Session chair: Atle Tangedal, Tekna	
15.30	**Creative technical solutions are just the first steps to success** Svenn-Tore Larsen, CEO, Nordic Semiconductor	
16.15	Closing words	
16.20	The end	

List of exhibitors:

- 4Test www.4test.no
- Arrow Norway (Altera) www.arrowne.com
- Avnet Memec (Microsemi/ prev. Actel) www.avnet-memec.no
- Avnet Silica (Xilinx) www.silica.no
- Bitvis www.bitvis.no
- EBV (Altera) www.ebv.com
- FirstEDA (Aldec) www.firsteda.com
- Informasic www.informasic.com
- Innofour (Mentor) www.innofour.com
- MathWorks www.mathworks.com
- Sigasi www.sigasi.com
- Synopsys www.synopsys.com
- vSync Circuits www.vsyncc.com

Price award (under middagen):

FPGA-Forum's price is given to the best FPGA related Master thesis in Norway.

The award committee: Knut Wold, Høyskolen i Gjøvik, Kjetil Ullaland, Universitetet i Bergen and Hans Jørgen Fosse, Mikrokrets AS.

De nominees in alphabetical order:

- Audun Wilhelmsen, NTNU:
  "Efficient Ray Tracing of Sparse Voxel Octrees on an FPGA"
- Leif Tore Rusten and Gunnar Inge Sortland, NTNU:
  "Implementing a Heterogeneous Multi-Core Prototype in an FPGA".
  (A joint thesis)
- Jonas Julian Jensen, UiO:
  "Reconfigurable FPGA Accelerator for Databases"

Entertainment (during the dinner party):

Studentkoret Candiss (Student choir)

FPGA-forum Program-committee:

- Arild Kjerstad, Kongsberg
- Hans Jørgen Fosse, Mikrokrets
- Jan Anders Mathisen, Silica/Xilinx
- Jim Tørresen, Universitetet i Oslo
- Atle Tangedal, Tekna
- Espen Tallaksen, Bitvis Design

Titles and Abstracts for presentations at FPGA-forum 2013

(In company alphabetical order)

Company & Presenter	**Title & Abstract**
4Test Instruments (Agilent) Thomas Göransson	**Key Challenges in the analysis and design of high speed digital links** Measurement fundamentals - High speed serial links, eye diagrams & jitter breakdown - When digital signals in FPGA's reach Gigabit speeds, "unpredictable" becomes the normal state of things. The process of getting your project back on track starts with the best tools and methodology for the job. Agilent's high speed digital solution is a range of simulation and measurement tools that help you cut through the challenges of gigabit digital designs to visualize Signal Integrity issues from both sides of the design and test flow
Aldec	See FirstEDA
Altera	See Arrow
Arrow (Altera) Nikolay Rognlien	**Open CL in fpga** Altera's efforts with OpenCL programming for fpga has materialized in real products, and shows very good results in productivity and power-savings. This presentation will describe the concepts of OpenCL and walk through a live hw demonstration.
Arrow (Altera) Nikolay Rognlien	**FPGA with ARM processor system on-chip…** This presentation will provide an introduction to the Altera SoC's ARM Processor Subsystem, seen from the FPGA designers and System Architects viewpoint. - Interfaces - DMAs, - Interrupts, - Memory maps, - Caches, - Debug features - Etc.

Atmel Odd Magne Reitan	**SystemVerilog for Configurable Designs** In spring 2011 Atmel Norway started a project where one of the main goals was to make a flexible RTL code base for a microcontroller family. The numerous parts of the family should be supported just by configuration of the same RTL: • Which peripheral modules to use, the number of instances • Pad/pin connections • Size of memories An internal development board using Xilinx Virtex-II was used for prototyping of the digital part. We chose to evaluate SystemVerilog (IEEE std 1800-2009) for design, and pushed the language to the limit of the support of the CAD tools. The code base must be supported in all CAD tools in the flow: • RTL Simulation (Synopsys VCS) • Chip Synthesis (Synopsys Design Compiler) • FPGA Synthesis (Mentor Precision-RTL, Synopsys) • Formal Equivalence Check (Synopsys Formality) • C-model compilation for Atmel Studio (GNU Verilator) This presentation outlines the choises we made, and presents the challenges we had with tool support. Finally it gives some general advice on what parts of SystemVerilog that works, and to which extent RTL code should be made configurable. It also mentions experiences we have with chip projects using System Verilog for design in production.
Avnet Memec (MicroSemi) Peter Trott	**Smartfusion2 SoC FPGA** Microsemi's next-generation SmartFusion2 SoC FPGAs are devices that address fundamental requirements for advanced security, high reliability and low power in critical industrial, military, aviation, communications and medical applications. SmartFusion2 integrates an inherently reliable flash-based FPGA fabric, a 166 megahertz (MHz) ARM® Cortex™-M3 processor, advanced security processing accelerators, DSP blocks, SRAM, eNVM, and industry-required high-performance communication interfaces all on a single chip.
Bitvis Design Espen Tallaksen	**Achieving the right FPGA design quality – Could reviews save the day?** Some of the most important quality aspects of an FPGA are: a) Functional quality. Does the FPGA perform its intended tasks - for all corner cases – and with no hiccups? b) Ease of modification. How easy is it to modify the design or add functionality – during or after the initial design? c) Readability and understandability. How easy is it (especially for somebody else) to understand the design – e.g. for a handover Proper functional verification may help you a long way with the “soft” part of the functional quality, but not with the hardware-related issues like timing and clocking. Lint-tools may help detect some bad coding style and check coding conventions, but this is a very minor part of designing for modification, readability and understandability. Thus in order to achieve the right quality we need good walk-throughs and reviews. Unfortunately however, most reviews are close to useless. This presentation exemplifies some critical quality aspects and suggests solutions on how to handle these.
Cisco Ove Brynestad	**Erfaringer med System Verilog/UVM testbenker** System Verilog/UVM ser ut til å øke i popularitet etter at UVM ble standardisert og akseptert av simulatorleverandørene i 2011. Foredraget vil presentere praktiske erfaringer med å ta det i bruk for verifikasjon av VHDL moduler.

Cisco Tore Fleten	**System verifikasjon av FPGA IO** Fra personen som tegner kretskortet, utlegger og FPGA verktøyet, setter alle krav/ønske til hvordan IO'en skal være. Jeg vil gå igjennom hvordan vi har dette med egenutviklede script og hvilke fordeler dette har gitt oss.
Cisco Dagrun Røyrvik	**Altera versus Xilinx** Erfaring med overføring av eksisterende Arria design (Altera) over til Kintex (Xilinx). Erfaring/Vurdering fra konvertering, verktøy, FPGA resurs forbruk, timing, power,….
Data Respons Hans Christian Lønstad	**Providing Linux tool chains, kernel and build system for SoC based FPGAs** The emergence of ARM based SoC FPGAs rises demand for an efficient and robust SW development environment. A fitting candidate would be the YOCTO system which is proven on regular CPUs for multiple architectures. The concepts involved and practical use of this system will be presented.
Data Respons Håvard Pedersen Alstad	**Effektiv bruk av eksternt minne** Det er ofte behov for å kunne mellomlagre store datamengder på høy båndbredde i mange FPGA-baserte applikasjoner. Når det interne minnet i FPGA-kretsen ikke strekker til må man ty til eksternt minne. I denne presentasjonen ser vi nærmere på hvordan minnet kan utnyttes best mulig uten å måtte dykke helt inn i minnekontrolleren.
EBV Amar Abid-Ali	**QSys - Conquer FPGA Design Complexity with System-Level Integration** As design complexities grow, and project timescales shrink, time to market becomes of utmost importance. Altera QSys is the answer to your design challenges. By removing obstacles in designing complex systems, the QSys tool allows you to concur your next FPGA Design with relative ease.
FirstEDA / Aldec Ian Gibbins	**OS-VVM: High-Level VHDL Verification** When facing the challenging task of implementing Constrained Random Stimulus or Functional Coverage in their testbench, VHDL designers used to make a difficult choice between "reinventing the wheel" (writing appropriate code from scratch) and "using a square wheel" (using SystemVerilog for verification). Fortunately, there is now a third option available: Open Source VHDL Verification Methodology. OS-VVM is a set of VHDL packages that provide reliable, field-tested procedures and functions handling randomisation and functional coverage. This presentation will demonstrate the structure and use of OS-VVM packages, paying special attention to Smart Coverage that combines random stimulus and functional coverage to provide faster verification.
GE Vingmed/Healthcare Morten Haugen	**User experience designing a FPGA for transfer 5.5 GByte/s from an analog frontend, into a pc for digital processing.** **Using two PCIe 8 lane / gen-2 , via 50 cm cable** The talk will focus on user experiences designing the FPGA interfacing 192 A/D converted data streams to a PC via PCIe. About 5.5 GByte/s are transferred and processed, two equal FPGAs each using a 8 lane PCIe gen 2 for the interface. Theoretical peak transfer rate for one 8-lanes/gen-2 in one direction is 3,6GByte/s, so reasonable result achieved. Signal Integrity, measurements at 5 GT/s, PCIe re-drivers, FPGA design at high speed, window-7 blue screen and CDC are some key words.

Informasic Tryggve Mathiesen	**Design reuse of both HW and SW – The topic of verifying and designing hetrogenious systems with ARM CPUs and High level design Synthesis.** The finalization of IEEE 1735 - Secure IP - platform independent source code encryption, together with IP packager - a common way to deliver IP to end customer and now the industrial defacto standard solution for adding your/3rd party IP into your system ARM AMBA AXI bus interface will wipe out the difficulties of using IP in FPGA based Embedded systems. The session will cover how to build, how to verify IP at production stage based on ARM AXI and FPGA SOC - faster HIL - Hardware in the Loop verification. It will furthermore show what is needed to create deliverable IP, based on HDL and SW in a secure way - using Secure IP and IP packager. The new won ability to partition the system into HW or SW modules later, utilizing the spatial and the temporal parallelism in the algorithms can be made in an agile way with FPGA SOC. The session will show how C/C++ based design can be partition into efficient SW modules on ARM Cortex CPU, or when it is appropriate - automatic transformed into submodules that can be added to the CPU infrastructures as peripherals or accelerating coprocessor in FPGA based CPU systems. The efficientness of the HLS tools, the verification methodology as well as the ability to manage the full project in agile SCRUM methodology will be discussed. High Level Synthesis tools like Vivado HSL, ARM Cortex A9 based FPGAs and SCRUM for FPGA design is to redefine the system design! We will show how the delivered IP will be integrated, verified and implemented in the target FPGA SOC, with the smoothness of source code integration. Ones the market have got new trust in new IP model, the market can be booming. The session will show how the IP market can overcome the blockage - delivering details, easy verifyable blocks without revealing the design secrets making IP a profitable and smooth business model.
InnoFour (Mentor Graphics) Rick Stroot	**The impact of requirement traceability in safety critical designs** Requirement management and traceability is essential within a safety critical development process such as those used for automotive, medical, aerospace or military projects, but it is equally valuable for any hardware or software based design flow. This session introduces Mentor Graphics' ReqTracer, our tool to help manage and automate requirements traceability from specification through design, implementation and validation. We will present an overview of ReqTracer, demonstrate the impact analysis and reporting capabilities, and take a look at the new features of ReqTracer 2012.1 to manage requirements at a system level. We will describe how ReqTracer fits into a team environment and show how its flexibility can trace requirements throughout many different tools and engineering flows.
Kongsberg John Aasen	**Designing and constraining Clock Domain Crossings** Errors caused by faulty clock domain crossing are intrinsically difficult to debug, since they are intermittent and dependent on as device, supply voltage, temperature (PVT), internal routing and aging. Simulation or lab-test cannot show that there are no CDC issues in a design. The CDCs need to correct by design. Guidelines for design and constraints of single-bit and multi-bit CDCs are needed. This presentation will show the CDC guidelines that are being developed at Kongsberg Defence Systems.
Kongsberg Norspace Espen Flo Eriksen	**FPGA i satellitt, demodulasjon i Command Receiver** Kongsberg Norspace utvikler for tiden neste generasjon av sin Command Receiver til bruk i satellitt. I denne benyttes FPGA til demodulasjon . En Command Receiver står for demodulasjon av signalene som inneholder kommandoer fra bakkestasjonen til satellitten. Det er således en kritisk komponent i en satellitt og det er vanlig med to eller flere slike mottagere om bord. Vi vil gi en beskrivelse av funksjonene som dette FPGA-designet inneholder og oppgavene det skal løse. Deretter vil vi fortelle om noen spesielle utfordringer knyttet til design av romkvalifisert elektronikk.
Mathworks Jonas Rutström	**Implementing DSP Algorithms on FPGAs using MATLAB and Simulink** We will present a single integrated workflow for speeding up the implementation and verification of algorithms in FPGAs and ASICs. Using real examples, you will gain insight into using the Model-Based Design methodology for developing algorithms for hardware implementation.
Mentor Graphics	See Innofour

MicroSemi	See Avnet Memec
Nordic Semiconductor Svenn-Tore Larsen	**Avslutningsforedrag : Svenn-Tore Larsen, Nordic Semiconductor** **Creative technical solutions are just the first steps to success**
NTNU Bahram Najafi-Uchevler	**Assertion Based Verification in Dynamic Reconfigurable Systems Using Functional Abstractions** Functional HDLs are an advantageous choice for verification and system level descriptions of complex electronic designs. We use high-level structures and concepts like higher-order functions, parameterisation, and partial evaluation from Haskell for describing dynamically reconfigurable circuits for FPGA's. Assertion-based verification hardware can be added to an FPGA design at run time, and for this we use Haskell for describing PSL-like properties and sequences. Both functional and verification HW is turned into RTL level VHDL with the CLaSH tool.
NTNU Milica Orlandić	**An efficient hardware architecture design for H.264/AVC intra prediction reconstruction path using dynamic partial reconfiguration** An increasing number of real-time video applications have created the need for higher coding efficiency. The H.264/AVC standard has a significantly higher compression performance and provides reduction in bitrate versus older standards MPEG–2, H.263 and MPEG–4. The objective is to build a platform for an autonomous, on-demand transcoding system and thus provide video decoding on mobile clients with minimal energy consumption. The dynamic partial reconfiguration is employed for modules such as quantization and inverse quantization in order to save area and ensure the high throughput.
Sigasi Philippe Faes	**Understanding legacy code** Still, there is much value in reading and understanding code. In fact, code comprehension is a very common activity for software developers and for hardware designers alike. It is practiced when fixing a bug, when a new person joins a design team, or when a team picks up old legacy code in order to reuse it in a new product. Still, understanding code is not an easy task. Perhaps if you wrote the code, you might remember some things. If the code is five years old, or if somebody else wrote the code, there is no way your recollection will be very useful. The coding conventions of the code under inspection may be quite different from what you are used to, or there might even be no code conventions at all. If you can’t rely on your memory and you cannot rely on coding conventions, which tools will you use to dig through a big pile of legacy code?
Sigasi Philippe Faes	**What FPGA designers can learn from the software guys** Obviously, hardware is older than software. In the old days all electronic circuits and all software was designed using pen and paper. Modern day design, based on computer languages was invented for software development and has only later been adapted by hardware designers. Given this head start, the software engineering community has created great tools. Revision control systems, instant feedback, issue trackers, and so forth. It may look like a big task to roll out all of these tools to a hardware design team. Especially small teams might feel that they would not benefit from tools and processes that could be associated with large corporate development teams. The truth is that all of those tools are easily available, even to a one-man team. With a development environment based on the Eclipse platform, you can access revision history, tickets and much more with the click of a mouse. This talk introduces an Eclipse-based tool set and development process.

Synopsys Antti Innamaa	**FPGA SoCs – A Centerpiece for Digital Design** SoCs have been the rage in ASIC markets for years, but are now becoming common in FPGAs with a soft core or external processor as the CPU. FPGA vendors estimate that approximately 50 percent of FPGA designs are integrated with CPUs in some way. Moreover, due to the advancement of FPGA technology itself, high-end silicon can capture extremely complex designs integrating a diverse range of IP, DSP and SW functionality. Naturally, as designs evolve, so must the tools and methodologies that are used to create them. Synopsys has been at the forefront of this wave of development and this presentation is an elaboration of new and innovative High-Level Design, FPGA and Hybrid Prototyping tools and methodologies that empower ASIC and FPGA designers of todays "digital design frontier".
Tabula Dennis Segers	**Keynote: Dennis Segers, Tabula** **Programmable logic technology; Enabling a "Renaissance of Innovation"** We live in a fast-paced world, with a sense that a continuous acceleration of technology innovation is the engine that drives it all. Contrary to this intuition, some recent studies suggest that the rate of innovation, at lease on a per-capita basis, is in steep decline. It is simply becoming too hard and too expensive. The world of chip design is indeed a microcosm of this trend as escalating expense and design complexity are resulting in a rapid decline in advance tape-outs and, more recently, a decline in chip startup funding. This presentation will examine these trends and discuss the role of programmable logic technology, coupled with innovative business models, as a means of reversing them.
vSync Circuits Reuven Dobkin	**Integration and Verification of Multiple-clock Domain FPGA Designs** Synchronization failures are a common pitfall in multiple clock domain designs. These bugs are hard to fix because the failures are often intermittent and hard to catch. Fixing such bugs in FPGA may take weeks of debugging, leading to long and unknown time-to-market. The problem is exacerbated by the fact that the synchronization bugs can be possibly generated by an incorrect automatic design optimization during synthesis and P&R stages, especially for designs having high area utilization, leading to low reliability designs. During the lecture we will survey common synchronization problems that arise during a design that targets a FPGA device. The survey will cover different design stages, starting from the RTL design using FPGA IP modules and down to synthesis, P&R and gate-level verification stages. In addition, we will suggest and discuss possible solutions to the presented problems at each one of the design stages. We will present a possible design methodology, leading to high reliability designs and to a shorter time to market, minimizing the time spent on synchronization bug fixing during lab testing.
Xilinx Olivier Tremois	**Xilinx - Enabling New Product Innovations Across Markets with Zynq SoC and Vivado HLS** Xilinx's Zynq™-7000 All Programmable SoCs are processor-centric platforms that offer software, hardware and I/O programmability. Combining a ARM® Cortex™-A9 multicore processor unit with advanced 28nm programmable logic and a portfolio of common AXI4 compliant IP, they enable higher performance hybrid processing systems with fewer devices, faster. This presentation will outline the core capabilities of Zynq All Programmable devices and in collaboration with emerging design tools, discuss how it can help address the needs of today's high performance hybrid systems : letting designers leverage the advanced integration whilst minimising time to market challenges. Whether you work in wireless, medical, defence, consumer or other – your likely using advanced algorithms that are more sophisticated than ever before. Xilinx's Vivado High-Level Synthesis accelerates IP creation by enabling C, C++ and System C specifications to be directly targeted into Xilinx All Programmable devices without the need to manually create RTL. Finally, a worked example of how to take a sophisticated algorithms and quickly and efficiently produce a custom, AXI4 compliant, hybrid design for Zynq All Programmable Soc will show all concepts in action.