FPGA forum

FPGA-forum 2024

The 17th FPGA-forum – where the Norwegian FPGA community meets

- FPGA-forum and exhibition: Wednesday 14th and Thursday 15th February 2024

At Royal Garden Hotel (Trondheim)

FPGA-forum er den årlige møteplassen for FPGA-miljøet i Norge. Her samles FPGA-designere, prosjektledere, tekniske ledere, forskere, siste års studenter og de største leverandørene på ett sted for 2 dagers fokus på FPGA.

Det blir foredrag fra norske bedrifter om utviklingsmetodikk og praktisk erfaring, universitetene presenterer nye og spennende prosjekter, og leverandørene stiller med aktuelle tekniske innlegg med et minimum av markedsføring. På utstillingen vil du kunne vurdere teknologi, verktøy og tjenester fra de ledende aktørene i bransjen.

FPGA-forum byr i tillegg på en ypperlig anledning til å møtes og utveksle erfaring innenfor FPGA-miljøet i Norge - både i pausene og under det sosiale arrangementet på kvelden.

In English:

FPGA-forum is a yearly event for the Norwegian FPGA community. FPGA-designers, project managers, technical managers, researchers, final year students and the major vendors gather for a two-day focus on FPGA.

There will be presentations from the Norwegian industry about methodology and practical experience, - the universities will present new and exciting projects, and the vendors will have technical presentations with a minimum of marketing. At the exhibition, you can evaluate tools and technology from the leading vendors.

FPGA-forum also provides an excellent opportunity to meet and exchange experience with the Norwegian FPGA-community – during the breaks – and during the official dinner party on Wednesday.

We are back on track – February every year 😊

Programme Wednesday, 14 February, 2024 (See abstracts below)

(Flags show spoken language. means English on request. Slide language is normally the same as the title. If in doubt check appendix.)

09.00	Registration and coffee	
Session 1	**Track AB**	
09.20	**Opening** (by Jim Tørresen, UiO and Espen Tallaksen, EmLogic)	
09.30	**Keynote by Thomas Preusser, Principal Engineer and Heterogeneous Digital Systems Research Engineer at AMD** (Introduced by: Arild Kjerstad, Kongsberg	
10.30	**Vendor presentations** (3 min. per exhibitor - in alphabetical order) (Chaired by: Espen Tallaksen, EmLogic)	
11:10	**Coffee break (and exhibition)**	
Session 2	**Track A** Session chair: Arild Kjerstad, Kongsberg	**Track B** Session chair: Åshild Ludvigsen, Appear
11.40	**40 years of Electronic Toll Collection: Use of FPGAs at Q-FREE** Svenn Bjerkem, Q-FREE	**Leveraging Open Source Frameworks in Commercial FPGA Development: A Case Study with SpinalHDL** Krzysztof Czyż, Embevity
12:10	**A satellite payload for handling high-speed data using Xilinx UltraScale+ RFSoC** Christophe Coutand, WideNorth	**FPGA innovation with RISC-V** Brian Colgan, Microchip
12:40	**Lunch and Exhibition**	
Session 3	**Track A** Session chair: Johan Alme, UiB	**Track B** Session chair: Åsmund Braathen, EmLogic AS
14:00	**Industrial Edge Applications with OPC/UA and robotics** Brian Colgan, Microchip	**Simulation Performance – Tips and Tricks** Sverre Vigander, Inventas
14:30	**Low Power and High Performance for Edge Applications - and beyond** Joachim Müller, Efinix	**Bugs Be Gone: Maximizing Early Bug Detection with Questa Design Solution in CI flow** Faïçal Chtourou, Siemens
15:00	**How simple graphs can yield deadlock free designs** Tom aan de Wiel and Simon Høgås, ARM	***Python testbenches in FPGA teaching at UiO*** Yngve Hafting, UiO
15:30	**Exhibition and Coffee**	
Session 4	**Track A** Session chair: Arild Kjerstad, Kongsberg	**Track B** Session chair: Jim Tørresen
16:00	**Intel Agilex® 5 FPGAs - Overview and Features** Nikolay Rognlien, Arrow	**Presentasjon av Masteroppgaver (For FPGA-forums pris for beste Masteroppgave 2023)**
16:30	**(No presentation)**	
17:00	**End of today's presentations**	
19.30	Aperitif TBD, Royal Garden Hotel	
20.00	Dinner party, Royal Garden Hotel. Including dinner entertainment with Pirum	

Programme Thursday, 15 February, 2024 (See abstracts below)

(Flags show spoken language. means English on request. Slide language is normally the same as the title. If in doubt check appendix.)

Session 5	**Track A** Session chair: Per Gunnar Kjeldsberg, NTNU	**Track B** Session chair: Heidi Skaar Johannessen, Norxe
09.00	**Good practice in teaching digital system design?** Yngve Hafting, UiO	**FPGAs and security on OSI layers 2, 3, and 4 - examples of MACsec, IPsec, and TLS implementations** Matti Tommiska, Xiphera
09:30	**Lens Flare Attenuation Accelerator Design with Deep Learning and High Level Synthesis** David Fosca Gamarra, TI	**Intel Agilex® 5 FPGAs - your Root-Of-Trust** Mark Frost, Intel FPGA
10:00	**The ABCs of AXI4: A Beginner-Friendly perspective** Christoffer Boothby, EmLogic	**European Cyber Resilience Act and its impact on IEC62243 and embedded system security** Paul Hardy, Lattice
10:30	**Exhibition and Coffee**	
Session 6	**Track A.** Session chair: Eivind Vågslid Skjæveland, HVL	**Track B** Session chair: Heidi Skaar Johannessen, Norxe
11:00	**Design of an FPGA based readout system for a detector-system at CERN** Tea Bodova, UiB	**DSim Cloud, GOWIN or go home?** Arild Velure, Inventas
11:30	**Lattice Avant-G and Avant-X: Bringing High Performance Serial IO and low power FPGA innovation to mid-range applications** Paul Hardy	**Get the right FPGA quality through efficient Specification Coverage (aka Requirement Coverage)** Espen Tallaksen, EmLogic
12:00	**Lunch and Exhibition**	
Session 7	**Track A** Session chair: John Aasen, Kongsberg	**Track B** Session chair: Magnus Jahre, NTNU
13:15	**Small-satellite payloads for spectrum monitoring** Eirik Grimstvedt, FFI	**Exploring the AMD Adaptable Intelligent (AI) Engine Architecture and Applications** Baha Hashimi, AMD
13:45	**FPGA Accelerated SRT** Åshild Ludvigsen	
14:15	**Coffee break**	
Session 8	**Track AB: Closing Keynotes** Session chair: Per Gunnar Kjeldsberg, NTNU	
14:45	**Closing Keynote: Roger Birkeland, NTNU Small Satellite Lab** Small Satellites at NTNU; How a university can work on what was earlier NASA's domain	
15:30	**Closing Keynote: Kyrre Lohne, KDA (Kongsberg)** Kongsberg Gruppen, Norwegian-developed technology and world leading solutions through 200 years. Innovation power and strategies to lift Norwegian industry into the future	
16:15	Closing words	
16:20	The end	

Keynotes:

- Opening keynote: Thomas Preusser,
  Principal Engineer and Heterogeneous Digital Systems Research Engineer at AMD.
  'Pervasive and Sustainable AI with Adaptive Computing'
  In the context of AI, we face a plethora of challenges that extend beyond the widely discussed performance scalability required to meet the growing demands of compute and storage in the latest models. These challenges encompass sustainability, pervasiveness, agility, and diversity, all of which are needed to cater to a constantly evolving range of applications and algorithms from endpoint to edge and cloud. In this talk, we explore how adaptive devices and agile compiler stacks can provide solutions by delivering post-production hardware specialization and co-designed algorithms. This results in highly optimized AI systems which not only provide the necessary performance scalability but also bring a reduction in carbon footprint while addressing the needs of a broad range of diverse applications with the necessary agility.

  Thomas is a principal engineer and the FINN project lead at AMD Research. Thomas earned a PhD from TU Dresden in 2011. He worked as a postdoctoral researcher both there and at ETH Zürich. He also enjoyed an EU-funded Individual Maria-Skłodowska-Curie Fellowship at the Xilinx Research Labs in Dublin. His scientific background is computer arithmetic, application acceleration and systems design using FPGAs. His current focus lies on advancing FINN, a tool for the generation of custom embedded neural-network inference solutions.

- Closing keynote Day 2:
  Kyrre Lohne, Vice President, Government Relations and Business Development, KDA
  'Kongsberg Gruppen, Norwegian-developed technology and world leading solutions through 200 years. Innovation power and strategies to lift Norwegian industry into the future.'
- Closing keynote Day 2:
  Roger Birkeland, NTNU Small Satellite Lab
  'Small Satellites at NTNU; How a university can work on what was earlier NASA's domain'

Price award for Best FPGA related Master thesis in Norway:

FPGA-Forum's price is given to the best FPGA related Master thesis in Norway.

The award committee:

- Dag Andreas Hals Samuelsen, University College of Southeast Norway, USN
- Geir Åge Noven, KDA
- Johan Alme, UiB

The nominees in alphabetical order:

- Lars Murud Aurud:
  "Improving Fetch and Issue Bandwidth in the Vortex GPU"
  Supervisor: Magnus Jahre
  Department of Computer Science, NTNU
- Samuel Boyle:
  "Design Space Exploration of FPGA Accelerators for Hyperspectral Anomaly Detection"
  Supervisor: Milica Orlandic
  Department of Electronic Systems, NTNU
- Jacob August Rangnes:
  "Hardware Acceleration of Real-Time Angle of Arrival Positioning"
  Supervisor: Per Gunnar Kjeldsberg and Karl Emil Sandvik Bohne
  Department of Electronic Systems, NTNU

All nominees will present their Master thesis in session 4B on day 1.
The winner will be announced during the dinner party.

List of exhibitors (for Wednesday and Thursday):

- Arrow Norway 1 (Intel) www.arrow.com
- Arrow Norway 2 (Lattice) www.arrow.com
- Avnet Silica (AMD/Xilinx) www.avnet-silica.com.
- Efinix www.efinixinc.com
- EmLogic www.emlogic.no
- InnoFour (Siemens EDA) www.innofour.com
- Kongsberg Discovery www. kongsberg.com/discovery
- Lightside Instruments www.lightside-instruments.com
- Microchip www.microchip.com
- Synective Labs www.synective.se
- Xiphera www.xiphera.com

KONGSBERG

Synective Labs

Workshops/Tutorials Day 0, Tuesday 13 February:

FPGA-forum workshops are handled 100% by each workshop organiser.

Workshop 1:
In connection with FPGA-Forum 2024 in Trondheim (14. – 15. February) Avnet Silica would like to invite conference participants to attend a whole day multi themed Workshop targeting AMD (Xilinx) technology and tools. The following themes will be covered through presentations and demos during the Workshop:

- An overview and update on AMD device and tools technology for FPGA/SoC designs
- Vitis Unified Software platform development – beyond traditional SDK functionality – AI and Application acceleration
- AMD High performance adaptive compute/Hardware design considerations
- Vitis AI and AI model deployment on KRIA KV260 Vision SOM
- An introduction to the new Microblaze RISC-V soft processor for current and future device technologies
- PYNQ Framework Composable data pipeline
- Q&A

The workshop will be delivered by Baha Hashimi and Jan Anders Mathisen (Avnet Silica) and Tryggve Mathiesen (AMD). Content will be delivered in English.

At lunch time Avnet Silica will serve pizza – coffee, tea and soft drinks will be available throughout the day. If you have any dietary restrictions - please advise Avnet Silica.

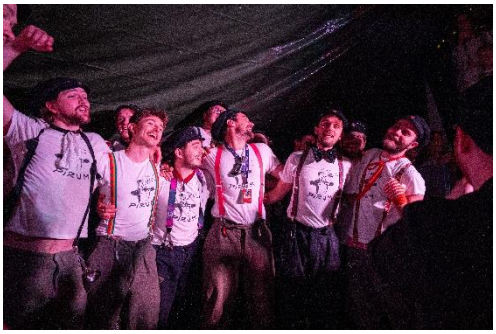
The Workshop is scheduled 13th February – 09:30-16:00 and will take place at the main campus of Norwegian Institute of Technology in Trondheim – not far from the FPGA-Forum venue (Royal Garden Hotel). More details will be provided to attendees.

Workshop is free of charge but requires registration in advance.

Seats are limited so please sign up as soon as possible by sending an e-mail to:

Jan Anders Mathisen, jananders.mathisen@avnet.eu, +47-91342393

Entertainment (during the dinner party): Pirum



UKEkoret Pirum is an all male choir from the student society Studentersamfundet in Trondheim. This untraditional choir is known for their charismatic show, silly outfits and spectacular vocal harmonies. Through their charm they've won hearts all over Trondheim, and contribute with humorous song and stage-show during the renowned student festival UKA. They are the quintessential student, living the student life to the fullest by their motto "The sun never sets for life's jolly boys"

FPGA-forum Program-committee:

- Arild Kjerstad, Kongsberg
- Heidi Skaar Johannessen, Norxe
- Jan Anders Mathisen, Silica/Xilinx
- Jim Tørresen, University of Oslo
- Per Gunnar Kjeldsberg, NTNU
- Espen Tallaksen, EmLogic

Titles and Abstracts for presentations at FPGA-forum 2024

(In company alphabetical order)

Note that written and oral presentations may be in English or Norwegian. Some presenters may also switch to English on Request
Presentations are thus marked 'Written' or 'Oral' and E (English), N (Norwegian) or EoR (English on Request)

Company & Presenter	Title & Abstract
AMD / Xilinx Thomas Preusser *Written: E,* *Oral: E*	***** Opening Keynote ***** **Pervasive and Sustainable AI with Adaptive Computing** In the context of AI, we face a plethora of challenges that extend beyond the widely discussed performance scalability required to meet the growing demands of compute and storage in the latest models. These challenges encompass sustainability, pervasiveness, agility, and diversity, all of which are needed to cater to a constantly evolving range of applications and algorithms from endpoint to edge and cloud. In this talk, we explore how adaptive devices and agile compiler stacks can provide solutions by delivering post-production hardware specialization and co-designed algorithms. This results in highly optimized AI systems which not only provide the necessary performance scalability but also bring a reduction in carbon footprint while addressing the needs of a broad range of diverse applications with the necessary agility.
Appear Åshild Ludvigsen *Written: E,* *Oral: E*	**FPGA Accelerated SRT** Secure Reliable Transport (SRT) is an open-source video transport protocol that utilizes the UDP transport protocol. SRT has typically been implemented using server-based solutions. Appear has utilized FPGA acceleration to achieve a market leading product with significant increased performance with respect to total throughput, max rate per connection and the number of connections. The presentation will cover how this was achieved by careful design of what parts of the implementation is more effective in FPGA vs CPU, and the communication between the two devices.
ARM Tom aan de Wiel and Simon Høgås *Written: E,* *Oral: E*	**How simple graphs can yield deadlock free designs** Deadlock and starvation are the bane of any complex system. Using human language descriptions to reason about deadlocks in an ad-hoc fashion will only get you so far. Human language descriptions are ambiguous, and the resulting design can be fragile. We present an approach using simple graph analysis for analysing potential deadlocks and starvation cases, eventually proving absence of deadlocks and a systematic approach to handling starvation. The approach is based on the concept of dependency graphs. Typically, the graph is present already at the architecture level, and it is refined and extended as more and more micro-architecture details are added. The result is a design that is "deadlock free by construction", which avoids many hard to discover deadlocks late in the design process. The analysis is also used by testbenches to make finding unanalysed deadlocks much more likely. The Arm GPU cache subsystem team has successfully used this approach for more than 10 years, resulting in a *very* low count of deadlock errata.
Arrow (Intel FPGA) Nikolay Rognlien **Exhibitor** *Written: E,* *Oral: EoR*	**Intel Agilex® 5 FPGAs - Overview and Features** Intel delivers a family of low power, high performance and cost-efficient mid-range FPGAs! Attend this session to find out more about the family, its roll-out through 2024 and see the first devices in action on a low-cost development kit from Arrow.

Avnet Silica / AMD Baha Hashimi **Exhibitor** *Written: E,* *Oral: E*	**Exploring the AMD Adaptable Intelligent (AI) Engine Architecture and Applications** The AMD AIE is a novel and key functional block present in many of the Versal device families as well as the new AMD Ryzen AI series of processors. The AIE and its infrastructure is a very capable but complex addition to the familiar AMD FPGA/SoC device primitives. The AI Engines are hardened ASIC DSP engines providing significant compute performance for machine learning inference and advanced digital signal processing applications. This session will introduce the following: - AMD AI-Engine architecture - AI Engines programming on different devices for multiple application use cases - Mapping of Artificial Intelligence models and compute intensive Digital Signal Processing algorithms onto AMD AI Engines platform. - AI Engine performance for multiple applications use cases. - Introduction to AI Engine development tool for developing AI applications and compute intensive acceleration applications on AI Engines.
Efinix Joachim Müller **Exhibitor** *Written: E,* *Oral: E*	**Low Power and High Performance for Edge Applications - and beyond** Titanium FPGA family is the second-generation FPGA introduced by Efinix Inc, Cupertino (California). While the first generation is used in many products already, Titanium consistently continues the path of solving special requirements not only but especially for edge applications. Among those requirements are size, power consumption, support for certain functions. The presentation takes a tour through Titanium general features and the specific ingredients as of today. To assess why Titanium is a good choice for the edge and beyond the presentation will conclude with an insight into power consumption, and an up-to-date snapshot of latest and upcoming expansions in terms of new features and new devices.
Embevity Krzysztof Czyż *Written: E,* *Oral: E*	**Leveraging Open Source Frameworks in Commercial FPGA Development: A Case Study with SpinalHDL** In the world of FPGA engineering, SpinalHDL stands as a versatile open-source framework. This presentation explores our experience with SpinalHDL in commercial projects, offering an assessment of its strengths and limitations. While SpinalHDL is not without flaws, it proves to be an exciting choice for FPGA engineers, underpinning our belief in its potential. We demonstrate the practical use of the discussed framework and highlight the need for improvements. Practical application is central to our presentation, where we illustrate how we've harnessed SpinalHDL in two distinct commercial projects. One project revolves around fiber optic sensing, while the other focuses on a quantum key distribution system. The framework was used in vital components of these system architectures, including 1 Gigasample ADCs, DACs, and a custom DMA engine. Additionally, we present our experience with VexRiscv, the soft-core RISC-V CPU implementation in SpinalHDL
EmLogic Christoffer Boothby **Exhibitor** *Written: E,* *Oral: EoR*	**The ABCs of AXI4: A Beginner-Friendly perspective** The AXI (Advanced eXtensible Interface) protocol has witnessed widespread adoption within the commercial FPGA (Field-Programmable Gate Array) market, garnering usage from both vendors and internal applications. Despite its complexity, comprehending the standard and extensive range of features associated with AXI can pose a challenge, especially for individuals transitioning from student status or those accustomed to others bus architectures such as Wishbone. Delving into the fundamental aspects of the AXI 4 protocol, this presentation aims to empower its audience with an understanding, enabling the development of more sophisticated systems utilizing the AXI protocol.
EmLogic Espen Tallaksen **Exhibitor** *Written: E,* *Oral: EoR*	**Get the right FPGA quality through efficient Specification Coverage (aka Requirement Coverage)** Specification coverage is getting more and more attention, and is critical for safety (e.g. DO-254) and mission critical (e.g. ESA space) applications. Unfortunately, this is often handled manually, which is really time-consuming and error-prone. UVVM's Specification coverage allows a very efficient collection of predefined requirements, and it generates the reports you need for both mission-critical and safety projects, and in fact for any project where quality is important. This presentation gives a brief overview of Specification Coverage before going into more details of proper Requirements Tracking. It also shows what is provided with UVVM and how this could be applied. UVVM is free and Open Source, and so are all the interface models, randomisation, functional coverage and specification coverage..

FFI Eirik Grimstvedt *Written: E,* *Oral: E*	**Small-satellite payloads for spectrum monitoring** FFI and partners launched the NorSat-3 and SMART MilSpace2 missions in April 2021 and January 2023 respectively. These are micro/nano-satellites that operate in low earth orbit and carry R&D payloads for spectrum monitoring purposes, specifically aimed at improving maritime safety. Both payloads are wideband, custom-built SDR platforms designed around the Zynq UltraScale+ MPSoC family from Xilinx. This talk presents an overview of the payload system-architecture at large, as well as some of the test and verification steps undertaken to successfully deploy and operate complex COTS hardware in space.
InnoFour	See Siemens EDA
Intel FPGA Mark Frost **Exhibitor** *Written: E,* *Oral: E*	**Intel Agilex® 5 FPGAs - your Root-Of-Trust** Intel's Agilex family of FPGAs contain a Secure Device Manager (SDM), a hardened root-of-trust and high-performance security engine (and key storage) which can be used to help secure your intellectual property from theft or modification. Attend this session to find out more about how to secure your designs.
Inventas Arild Velure *Written: E,* *Oral: EoR*	**DSim Cloud, GOWIN or go home?** As the clouds are gathering all around us, we take a peek above them and gander at these newfangled things, are they the emperor's new clothes. For this presentation we will have a look at simulation as a service (SaaS), with a focus on the new arrival DSim Cloud, a VHDL/SV cloud-only simulator from Metrics Design Automation. GOWIN, the relatively new FPGA vendor, has a collaboration with them, so we take the opportunity to use a GW1NR-9 FPGA chip as the test subject.
Inventas Sverre Vigander *Written: E,* *Oral: EoR*	**Simulation Performance – Tips and Tricks** Abstract: Verifying modern FPGA designs is complicated and time consuming, and verification coverage is often limited by your ability to run simulations. Full verification requires many test cases, and when the test suite grows, so does the time it takes to run your regression. Learn some tricks to reduce your simulation time, to get the most out of the simulations and spend less time waiting for results!
KDA Kyrre Lohne *Written: E,* *Oral: E*	***** Closing Keynote ***** **Kongsberg Gruppen, Norwegian-developed technology and world leading solutions through 200 years. Innovation power and strategies to lift Norwegian industry into the future** Kongsberg is an international, knowledge-based group that supplies high-tech systems and solutions to customers in the energy, merchant, navy and defence and aerospace industries. Kongsberg has more than 13,000 employees in 39 countries and had total revenues of NOK 31.8bn in 2022. The company is experiencing strong growth and has extensive collaboration with academia to motivate young people to choose technology and science subjects, and carries out an extensive recruitment program to hire up to 5,000 new employees over the next 5 years.
Lattice Semiconductor Paul Hardy **Exhibitor** *Written: E,* *Oral: E*	**European Cyber Resilience Act and its impact on IEC62243 and embedded system security** Many nation states and collectives of them are now embracing the concepts of Cyber Resilience. The most recent example is the European Commission's Cyber Resilience Act. Prior to this, the United States National Institutes of Standards and Technology (NIST) had published a seminal guideline with the NIST Special Publication 800-193, entitled Platform Firmware Resilience which is not a de-facto standard applied to all major Hyperscaler Servers. This summer the Trusted Computing Group (TCG) released their Cyber Resilient Module and Building Block Requirements. In this paper we will highlight how using strong Root of Trust (RoT) FPGA technologies can help implement best practices with regards to CyberResilient Systems to meet the coming compliance implementations from the EC Cyber Resilience Act, as well as NIST SP 800-193 Platform Firmware Resilience Guidelines and the TCG Cyber Resilient Module and Building Block Requirements. Topics covered will include the fundamental Protect-Detect-Recover cycle of Cyber Resilient Systems and how best to implement such a cycle using RoT FPGA technologies which are well suited for demands of a real-time cyber resilient system. Additionally, the security paradigm change concepts that Cyber Resilience is ushering will be detailed. Such as the required mindset change from avoiding a cyber attack to accepting the high probability of attack and how to best operate through it with minimal to no damage (a fundamental of cyber resilience).

Lattice Semiconductor Paul Hardy **Exhibitor** *Written: E,* *Oral: E*	**Lattice Avant-G and Avant-X: Bringing High Performance Serial IO and low power FPGA innovation to mid-range applications** Built on the award-winning Lattice Avant platform, the Avant-G and Avant-X FPGA families offer power efficiency, advanced connectivity, and optimized compute for mid-range applications across the Communications, Computing, Industrial, and Automotive markets. Avant-G general purpose FPGAs are designed to enable a wide range of customer needs by offering seamless, flexible interface bridging and optimized compute for system expandability. Lattice Avant-G devices offer best-in-class signal processing and AI, flexible I/O supporting a range of system interfaces, while providing dedicated LPDDR4 memory interfaces at 2400 Mbps. Avant-X advanced connectivity FPGAs are designed to enable high bandwidth and security, with a feature set tailored to customer needs for signal aggregation and high throughput. Lattice Avant-X devices offer up to 1 Terabit per second total system bandwidth, PCIe® Gen 4 controllers with hard DMA, and a security engine to encrypt user data in motion providing quantum safe cryptography. Lattice will provide a full technical overview of these new devices.
Microchip Brian Colgan **Exhibitor** *Written: E,* *Oral: E*	**FPGA innovation with RISC-V** Microchip's FPGA business unit will explore the AI Edge requirements, and how new compute capabilities driven by RISC-V are shaping the future. In an ever-changing landscape, the edge demands new power-efficient technology, quantum threat protection, enhanced signal and image processing, and evolved development tool paradigms. Learn more about the latest RISC-V based programmable innovations and roadmap of the PolarFire® and PolarFire 2 Platform, bringing the future to you now.
Microchip Brian Colgan **Exhibitor** *Written: E,* *Oral: E*	**Industrial Edge Applications with OPC/UA and robotics** OPC/UA and ROS are gaining prominence in connected industries and robotics, respectively. This session demonstrates how to integrate these technologies for an industrial vision application using H.264 compression on an SoC-FPGA. We'll also highlight the latest PolarFire SoC dev kit, the BeagleV-Fire, running ROS, along with the PolarFire SoC video kit for showcasing these applications.
NTNU Small Satellite Lab Roger Birkeland *Written: E,* *Oral: E*	****** Closing Keynote ****** **Small Satellites at NTNU; How a university can work on what was earlier NASA's domain** The advent of the CubeSats in early 2000s has paved the way for many new actors in the space hardware community and industry. The CubeSats are "so simple that even a first-year student can make one". In this talk, we will take a look at some of the enablers for the success of the CubeSats, and then focus on the impact this has had for universities such as NTNU. NTNU has had CubeSat activities continuously for more than the past 20 years, with a big escalation since around 2017. A total of four satellites has been attempted launched. In 2022 both the HYPSO-1 research satellite and the student satellite SelfieSat were successfully launched and have since then had considerable success and impact both at NTNU, nationally and even internationally. In 2024 two new satellites are ready for launch. The hyperspectral instrument of the HYPSO-1 satellite will be presented in greater detail, focusing on both the mission idea and how an advanced optical payload, based on COTS components including FPGAs, could be built by PhD and master students in less than four years from idea to delivery, a pandemic included.
Q-Free Svenn Bjerkem *Written: E,* *Oral: EoR*	**40 years of Electronic Toll Collection: Use of FPGAs at Q-FREE** Q-FREE Norge AS is a Trondheim based, industry leading provider of equipment for Electronic Toll Collection (ETC) with 40 years of experience in this industry. We will present some highlights from our product development history of ETC equipment in the 5.8GHz DSRC band. We will also show how FPGAs are used both as a key component in the Road Side equipment and as verification tool for Q-FREE IPs in ASIC/ASPPs in our product portfolio. How we select, test and verify the FPGA behavior and how the FPGAs interact with other devices they maintain.
Siemens EDA / InnoFour Faïçal Chtourou **Exhibitor** *Written: E,* *Oral: E*	**Bugs Be Gone: Maximizing Early Bug Detection with Questa Design Solution in CI flow** This presentation focuses on empowering designers to enhance the quality of their code deliveries without the hassle of creating testbenches and conducting tests for every block. By ensuring high-quality designs, verifiers can focus on debugging more complex issues rather than trivial ones. Questa Design Solutions aims to assist designers in swiftly identifying issues, ensuring code repository stability, and improving the quality of deliveries to other teams. By integrating these tools into a continuous integration flow, automatic and regular code checks can be enabled, resulting in improved efficiency and greater schedule predictability through easily understandable metrics.

TI David Fosca Gamarra *Written: E,* *Oral: E*	**Lens Flare Attenuation Accelerator Design with Deep Learning and High Level Synthesis** Lens flare artifacts are undesired visual distortions caused by stray light, which can negatively impact the integrity and quality of an image. These artifacts pose a significant challenge in industrial applications like automotive and surveillance, where the quality and reliability of input images from cameras are crucial. Artificial intelligence, particularly deep learning neural networks, have shown promising results in attenuating lens flare. This talk presents work done for a master thesis at Department of Electronic Systems, NTNU, in cooperation with Sony Semiconductor Solutions Europe. A synthetic flare dataset is generated, and an iterative training process that includes evaluation of transfer learning is employed to develop FlareNet, the first compact and lightweight U-Net based model for lens flare reduction. To demonstrate the viability of using a model such as FlareNet as a hardware accelerator, the neural network is implemented in C++ using Vitis HLS. Synthesis and validation are performed using the Vitis tool, utilizing less than 20% of a Zeus Zynq UltraScale FPGA.
UiB Tea Bodova *Written: E,* *Oral: E*	**Design of an FPGA based readout system for a detector-system at CERN** We are currently in the phase of writing the design specifications for a new detector system at CERN. The ALICE Forward Calorimeter, or FoCAL in short, consists of three separate detector-systems, where we in Bergen is in charge of one of these systems; the electromagnetic pixel detector. The pixel detector consist of two planes of Monolithic Active Pixel Sensors (MAPS) of about 1 squaremeter each, that are squeezed in between the other parts of the detector. This gives about 255 million pixels divided into 3888 MAPS that must be powered, read out and controlled. When designing the electronics for this, we phase several challenges. First of all, the radiation environment is harsh, where both dose effects and single event effects is a possibility and must be mitigated by design or by careful selection of components. Secondly, due to the confined space 60 meters underground, special HSE regulations require that all cables used must be halogen-free, since standard cables release toxics in case of a fire. The third challenge is that the space for our 28 readout boards and 28 power controller boards are limited. We essentially have two options: (1) close to the detector, where the radiation environment is bad, but the length of cables from the detector are less than 5 meters, or 20 meters away from the detector, where the radiation level is closer to ground level, but the cables are so long that the signal quality is horrible. This talk will discuss how we plan to tackle these challenges, and why FPGAs are a mandatory part of this solution.
UiO Yngve Hafting *Written: E,* *Oral: E*	**Good practice in teaching digital system design?** In the period from 2018 to 2023 we have made several changes to our bachelor-level course in digital system design (IN3160/4160) to facilitate better understanding and coding of RTL designs. This has led to changed recommendations for good practice and code, such as using three-process state machines, separating register usage and combinational logic, etc. Despite immediate changes in lectures and books, it has taken considerable time to change practice among the students during their exam. In this presentation we will go through some concrete examples of recommendations and our experiences of what it takes to get results all the way to the end.
UiO Yngve Hafting *Written: E,* *Oral: E*	**Python testbenches in FPGA teaching at UiO** Following incremental changes in FPGA teaching the last few years, from the spring semester 2024 we will shift to using Python based testbenches in our bachelor course in digital system design (IN3160) at the University of Oslo. In the presentation we will present the rationale behind, practical considerations and challenges following these decisions.
WideNorth Christophe Coutand *Written: E,* *Oral: E*	**A satellite payload for handling high-speed data using Xilinx UltraScale+ RFSoC** A satellite payload that stores high speed data from other payloads and transmits the data to ground has been developed using an UltraScale+ RFSoC as the main processing unit. The payload can receive high-speed data streams of up to 20 Mbps over fiber as well as several lower-speed streams using electrical interfaces. The data streams are multiplexed into high capacity Solid State Hard Drives with a total capacity of 3.8 TB. The stored data is transmitted to ground station using a high-speed DVB-S2X radio supporting up to 5 Gbps datarate. The radio uses a 10W PA operating in Ka-band (25.5 - 27.0 GHz). Adaptive Coding and Modulation (ACM) is used to further improve the downlink throughput. The payload will operate in a LEO orbit with moderate radiation. The payload uses a Defence Grade Ruggedized UltraScale+ RFSoC (XQZU48DR). All power supplies are monitored by a Radiation Hardened ARM Cortex M4 micro controller from Vorago to detect and correct any harmful Single Event Latchup in the payload.

Xiphera Matti Tommiska **Exhibitor** *Written: E,* *Oral: E*	**FPGAs and security on OSI layers 2, 3, and 4 - examples of MACsec, IPsec, and TLS implementations** MACsec (Media Access Control Security), IPsec (Internet Protocol Security), and TLS (Transport Layer Security) are widely used security protocols for OSI (Open Systems Interconnection) model layers 2 (Data Link Layer), 3 (Network Layer), and 4 (Transport Layer) respectively. FPGAs can enhance the performance of tasks such as encryption, decryption, and cryptographic key management in these security protocols, thus making secure communication more efficient. This presentation will present real-life FPGA-based implementations of MACsec, IPsec, and TLS and will explore the similarities and differences between the three security protocols.