FPGA
forum

Preliminary programme per 25 Nov 2021

FPGA-forum 2022

The 16th FPGA-forum – where the Norwegian FPGA community meets

- FPGA-forum and exhibition: Wednesday 9th and Thursday 10th February 2022

At Royal Garden Hotel (Trondheim)

FPGA-forum er den årlige møteplassen for FPGA-miljøet i Norge. Her samles FPGA-designere, prosjektledere, tekniske ledere, forskere, siste års studenter og de største leverandørene på ett sted for 2 dagers praktisk fokus på FPGA.

Det blir foredrag fra norske bedrifter om utviklingsmetodikk og praktisk erfaring, universitetene presenterer nye og spennende prosjekter, og leverandørene stiller med aktuelle tekniske innlegg med et minimum av markedsføring. På utstillingen vil du kunne vurdere teknologi, verktøy og tjenester fra de ledende aktørene i bransjen.

FPGA-forum byr i tillegg på en ypperlig anledning til å møtes og utveksle erfaring innenfor FPGA-miljøet i Norge - både i pausene og under det sosiale arrangementet på kvelden.

In English:

FPGA-forum is a yearly event for the Norwegian FPGA community. FPGA-designers, project managers, technical managers, researchers, final year students and the major vendors gather for a two-day focus on FPGA.

There will be presentations from the Norwegian industry about methodology and practical experience, - the universities will present new and exciting projects, and the vendors will have technical presentations with a minimum of marketing. At the exhibition, you can evaluate tools and technology from the leading vendors.

FPGA-forum also provides an excellent opportunity to meet and exchange experience with the Norwegian FPGA-community – during the breaks – and during the official dinner party on Wednesday.

Titles and Abstracts for presentations at FPGA-forum 2022

(In company alphabetical order)

Note that written and oral presentations may be in English or Norwegian. Some presenters may also switch to English on Request
Presentations are thus marked 'Written' or 'Oral' and E (English), N (Norwegian) or EoR (English on Request)

NOTE: Presentations from the following will be included in a next version of the programme
- Arrow/Intel FPGA
- AvnetSilica/Xilinx

Company & Presenter	Title & Abstract
Aldec	See FirstEDA
Appear Egil Fykse *Written: E, Oral: E*	**Formal verification using open-source tools** We will present our experience with open-source formal verification tools. Bugs can be hidden in corner cases of the design that are not explored by the testbench, and formal verification can help find these bugs. This is a useful tool both for verification of new modules and bug hunting after a module has failed in the field. Some practical examples will be presented, as well as limitations of the tools.
ARM Nicola Vianello *Written: E, Oral: E*	**Highly efficient signal capture infrastructure for waveform extraction on FPGAs** A
Arrow (Intel FPGA) Nikolay Rognlien *Written: E, Oral: EoR*	**T** A
Arrow (Intel FPGA) Nikolay Rognlien *Written: E, Oral: EoR*	**T** A
Arrow (|Lattice) Renè Jensen *Written: E, Oral: E*	**Nexus Platform FPGA** New families of Low power FPGA's with four different family members. All made on the 28 nm FD-SOI process which gives lower power and higher reliability than competing FPGA. The FPGA's range from 11K to 96K Logic Cells and the families have different hard IP's likes: 10 Gbps MIPI CSI-2 DPHY, 5G PCIe Gen2, SGMII CDR, ADC, 10GE PCS, PCIe Gen3 and Security blocks with Crypto. Come and hear how this can benefit you and your company.

Arrow (Microchip) ? *Written: E, Oral: E*	**Microchip Multicore RISC-V based PolarFire® SoC platform – Linux & RealTime capable** Learn about Microchip's new PolarFire® SoC FPGA family innovative architecture, combining low power consumption, thermal efficiency with defense grade security for smart, connected systems able to address edge processing requirements for Industrial Automation, Automotive & Medical applications. It's the first system on chip (SoC) field-programmable gate array (FPGA) with a deterministic, coherent RISC-V CPU cluster enabling Linux and real-time applications.
AvnetSilica (Xilinx) Jan Anders Mathisen *Written: E, Oral: N*	**T** A
CERN Ola Grøttvik *Written: E, Oral: ?*	**Installation, integration and first operating experiences of the ALICE ITS Upgraded Readout System** The ALICE Inner Tracking System has gone through a significant upgrade for the upcoming third running period of the CERN LHC. The new detector consists of seven layers of high-granularity pixel sensors, and is the largest MAPS-based detector ever built with 10 m2 of sensitive area. 192 custom FPGA-based readout units control the sensors and transmit the data upstream for analysis. This contribution describes the current system focusing on the FPGA tasks, the system status and the expertise gained by moving from commissioning to the installation and throughout the data-taking preparation period, focusing on the intricate integration with other system components. Selected challenges, issues, and lessons learned during the various commissioning periods are presented.
EmLogic Andre Firing *Written: E, Oral: EoR*	**Functional Safety on FPGA** Digital systems have become vital in controlling and monitoring safety critical systems where a failure can result in catastrophic consequences. With predictable behavior and fast response time, FPGAs are well suited for these applications. However, making safety critical designs brings on a new set of challenges for the FPGA designer.
EmLogic Espen Tallaksen *Written: E, Oral: EoR*	**Enhanced Randomisation and Functional Coverage** UVVM released brand new functionality on Enhanced Randomisation and Functional Coverage in October last year. As always with UVVM, testbench readability, overview and user friendliness where it matters the most, are the highest priorities. This presentation will show you why and how, - and you will even get a mini course on Functional Coverage.
FirstEDA Nomita Goswami *Written: E, Oral: E*	**How can complex FPGA projects benefit from register automation?** As design complexity continues to increase, so does the number of registers residing on the HW/SW interface used to control the operations of the SoC/IP. The associated register definitions constantly evolve during the design cycle. A single register specification source means the required outputs can be automatically generated for the different teams. In this presentation we will introduce SystemRDL 2.0 and discuss why this register description language is a preferred method of describing SoC/IP registers. We will cover register specification capture and describe an automated path from the specification to supporting documentation, HDL creation and other files that support the software access to the APIs. We will also explore the ability to parametrise components further, to improve design re-use and talk about the benefits of automation.

GRIFF Aviation Svein Even Blakstad *Written: N, Oral: N*	***** Closing Keynote ***** **GRIFF, reisen fra en liten vestlandsfjord - ut i den store verden** GRIFF Aviation er en norsk droneutviklingsbedrift lokalisert i Sykkylven i Møre og Romsdal. De utvikler droner med løftekapasitet på 100 kg+. I dette foredraget tar utviklingssjef Svein Even Blakstad oss med på reisen som selskapet har vært gjennom og veien videre inn i fremtiden. Det blir fokus på milepæler oppnådd, utfordringer underveis og hvordan de har blitt løst.
HDL Works Willem Gruter *Written: E, Oral: E*	**Placing an FPGA on a board. Guidelines for efficient design/verification between FPGA and PCB environments** Developing hardware that involves an FPGA requires work in both an FPGA and a PCB design environment. They are separated environments but require close interaction. In this interaction there are different approaches and strategies possible. In my presentation I will outline guidelines, peculiarities of FPGA/PCB systems, useful naming conventions and explain why keeping a strict relationship between names on the FPGA and PCB will save you time and improve the quality of design.
HVL Simon Voigt Nesbø *Written: ?, Oral:?*	**Open-source radiation-tolerant CAN controller** The Controller Area Network (CAN) bus protocol defines a fault-tolerant multi-master serial protocol. Originally it was intended for use in vehicles, but the robustness of the CAN protocol has made it a popular choice in a wide range of control applications, also in the radiation environments seen in space applications or high-energy physics experiments. Electronics designed for radiation environments often feature an FPGA, and employ Triple Modular Redundancy (TMR) to achieve radiation tolerance. There are several varieties of TMR, and the best choice is highly technology-dependent. We are presenting a new open-source CAN controller written in VHDL for FPGAs. The controller is highly configurable, but when used in a radiation environment, it features TMR techniques specifically tailored for SRAM FPGAs.
HVL Svein Haustveit *Written: ?, Oral: ?*	**Undervisning i digitalteknikk, VHDL og FPGA ved Høgskulen på Vestlandet.** • Status • Min erfaring med å komme tilbake til undervisning etter 30+ år i industrien • Er det noe gamle «sirkusnummer» som kan tas ut? • Hva skal inn?
InnoFour	See Siemens EDA
Intel FPGA	See Arrow
Inventas Arild Velure *Written: ?, Oral: ?*	**Erfaring med oversetting av MIL-1553 testbenk fra TCL til UVVM** Legacy kode bygger seg ofte opp over tid, men noen ganger er det bedre å ta et tak og lede ting inn i nåtiden. I denne presentasjonen vil vi gå igjennom prosessen vi brukte for å oversette TCL testbenker til VHDL UVVM VIP, hindringer underveis og de endelige fordelene. Det som kan nevnes er en økning i simulerings hastighet, enklere integrering med UVVM specification coverage og kompatibilitet med GHDL, som så gjør det enklere å kjøre mange regressjonssimuleringer samtidig i CI.
Inventas Marius Elvegård *Written: ?, Oral: ?*	**UVVMs nye regresjonsverktøy** Et FPGA-design vil ofte ha et stort sett med tester som må kjøres for å verifisere funksjonaliteten. Et godt verktøy for effektiv og strukturert testing er derfor viktig. UVVM har nå fått et nytt regresjonsverktøy som er utviklet nettopp med tanke på dette; å effektivt kjøre konfigurerbare tester og å bygge en test-struktur hvor alle kjøreresultater er lett tilgjengelige.

KDA Steinar Christensen *Written: E, Oral: E*	**Toolbox for Safety critical design in RTL** In a safety critical design one should assume that everything can go wrong. Some error mitigations are done on the PCA level, and some are better suited for FPGAs. This presentation covers some concrete examples of how error mitigations can be implemented in safety critical systems.
Lattice	**See Arrow**
Lightside Instruments Vladimir Vassilev *Written: ?, Oral:?*	**Network Programmability kit for Ultra96** We needed a platform similar to NetFPGA but for newer Zynq Ultrascale+ families. With free development tools license for Vivado. With an option to connect GNSS disciplined timing source. We also wanted it to be robust and preferably in a 1U rack form factor. We also wanted it to be modular within the 1U dimension limits. And we wanted the management software for the cores to be 100% based on YANG/NETCONF. And the YANG model to be a published open standard. And we wanted the toolchain for this software to be part of Debian. We also wanted a well known application to demonstrate this platform. We implemented a RFC2544 benchmark in python using the YANG/NETCONF interface. We produced all the prototypes at Bitraf (Oslo). We made the hardware and software open-source.
Maxfield High-Tech Consulting Clive “Max” Maxfield *Written: E, Oral: E*	***** Opening Keynote ***** **TBD**
Microchip (FPGA)	**See Arrow**
Microchip Technology Johannes Wågen, Egil Rotevatn and Lloyd Clark *Written: E, Oral: E*	**FPGA emulation of a new USB peripheral for a microcontroller** Designing and validating a new USB peripheral for a microcontroller is challenging. The complexity of the USB protocol makes verification difficult. Simulations take a long time to run and require a USB host that is simulated accurately. In order to speed up and improve the quality of the validation process, a complete microcontroller including the new USB peripheral was emulated on an FPGA. This allowed us to validate the hardware design with software stacks when connected to real USB hosts on all major operating systems. It also allowed errors to be injected at a far higher rate than simulations allow and confirm that the design is robust. A standard Microchip debug and programming interface was included as part of the emulated microcontroller. This made it possible to use our standard software development tools such as Microchip Studio, and our Applications engineers could seamlessly perform software development and debugging just as if they had the finished production microcontroller in front of them. Software and hardware development could proceed in parallel, greatly tightening the schedule and allowing bugs to be found and fixed earlier. This presentation outlines the choices we made and the experiences we had throughout this project, as well as lessons learned that may be valuable to anyone using FPGA emulation to reduce the risk of hardware design.
Norbit Per Jørgen Weisethaunet *Written: ?, Oral:?*	***** Closing Keynote ***** **Er «Made in Norway» moderne igjen?** NORBIT har gått motstrøms og satset på både utvikling og produksjon i Norge. Adm.dir i NORBIT Per Jørgen Weisethaunet vil fortelle om NORBIT sin strategiske satsning og hvorfor de mener dette er en satsing for fremtida, krydret med eksempler på spennende prosjekter for norske selskap.

Novelda Espen Stenersen *Written: ?, Oral:?*	**Using FPGAs, Python, gRPC, and Azure DevOps to automate ASIC prototyping and testing** This presentation will talk about how Novelda is using an SoC FPGA board to test, validate, and characterize our Ultra-Wideband radar ASICs, using Python and gRPC to communicate with the board, and Azure DevOps to automate builds, testing and reporting. This platform enables an engineer to work connected or remote, and relaxes the computing and real-time requirements of a host communicating with a Novelda ASIC or prototyping FPGA.
NTNU Björn Gottschall *Written: ?, Oral:?*	**Cycle-accurate signal trace analysis on FPGA accelerated CPU simulations** We have developed a profiling framework which allows us to efficiently analyze signal traces inside a cycle-accurate FPGA accelerated hardware simulation. We use it to measure application performance during the execution of industry standard benchmarks in a full-stack Linux system on a high performance out-of-order RISC-V CPU. For the first time, we were able to measure the execution latency of all instructions within a processor down to the single cycle. Using this data we created a golden performance reference which tells exactly how much time each instruction, function and application has spent executing.
NTNU David Metz *Written: E, Oral: ?*	**Dynamic High Level Synthesis Based on the Regionalized Value State Dependence Graph** High-level synthesis (HLS) promises to improve developer productivity by raising the abstraction level. While statically scheduled HLS has been in use for a few years, and is an active field of research, it suffers from poor performance in control and irregular memory access heavy applications. The dynamic nature of these workloads also makes them difficult to accelerate using an RTL-based design process. HLS based on dynamically scheduled dataflow networks promises increased performance in these applications at the cost of a larger hardware footprint. Trading resources against performance is becoming increasingly favourable as the available resources on FPGAs, especially in the datacenter, are growing. We present an HLS framework for generating dynamically scheduled networks based on the regionalized value state dependence graph (RVSDG) intermediate representation. We further describe how the RVSDG's unified representation of control- and data flow can be easily translated into a dynamically scheduled dataflow network. We show that, for dynamic workloads, circuits generated using dynamically scheduled HLS outperform those generated by statically scheduled HLS.
Siemens EDA / InnoFour Faïçal Chtourou *Written: E, Oral: E*	**Using Python for a high-quality reusable verification environment.** Constrained randomization and functional coverage have recently become crucial elements to a successful verification of FPGA and ASIC design. SystemVerilog and UVM framework is the de-facto standard for verification. Still, due to a high learning time/benefit ratio, many users preferred to look into other alternatives such as UVVM/OSVM. Lately, Python has emerged as a third option, and it is gaining interest for its obvious advantages (easy language, big community, extensive library …) The purpose of this presentation is to show you how we can build a high-quality reusable verification environment using Python Libraries/Framework.
UiB Bendik Husa *Written:E, Oral:E*	**Experiences with NanoXplore's space-grade SRAM-based NG-MEDIUM FPGA** NG-MEDIUM is the first FPGA from the French company NanoXplore and it was made commercially available in 2018. This is a new and promising competitor in the range of available FPGAs for use in radiation-heavy environments. It is rad-hard by design, and produced in a rad-hard 65 nm CMOS process by STm. In addition, it features several mitigating techniques for radiation effects such as EDAC and a built-in and automatic configuration scrubber. It is the first European FPGA to be space qualified according to ESCC requirements in 2020, and as such the NanoXplore range is the only ITAR/EAR-free FPGA family of its kind. I will walk you through both the architecture of the FPGA and the design flow using NanoXplore's Python-based software suite NanoXmap. I will also talk about my experiences working with this FPGA in a real design.

WideNorth ? *Written: ?, Oral:?*	**High-end Software Defined Radio (SDR)** Presentation of the hardware design and the software framework for a powerful, modular SDR platform.
WideNorth ? *Written: ?, Oral:?*	**User Terminal Wideband Modem for Very High Throughput Satellites (VHTS)** Presentation of a DVB-S2X Modem prototype supporting data rates up to 5 Gbps / 1.4 Gsps.
Xilinx	See also Avnet Silica
Xiphera Matti Tommiska *Written: E, Oral: E*	**FPGAs and Post-Quantum Cryptography** Large-scale quantum computers will outperform classical computers in solving certain hard computational problems. Amongst these are RSA and elliptic curve discrete logarithm problem, which form the basis of contemporary public key cryptography underlying all Internet security. NIST (National Institute of Standards and Technology) is currently running a PQC (Post quantum cryptography) competition to standardize quantum-secure public key cryptosystems. The reconfigurability of FPGAs will play an important role in PQC adoption, as it will allow simultaneous support for both classical and PQC public key cryptography. Another distinct advantage of FPGAs is algorithm agility, which will enable continuous support for the most recent versions of the evolving PQC standards. The presentation will review the state-of-play of PQC standardization, and summarizes the current status of FPGA support for PQC algorithms.