FPGA forum

# FPGA-forum 2022

## The 16th FPGA-forum – where the Norwegian FPGA community meets

**- FPGA-forum and exhibition: Wednesday 7th and Thursday 8th September 2022**

**At Royal Garden Hotel (Trondheim)**

**FPGA-forum er den årlige møteplassen for FPGA-miljøet i Norge. Her samles FPGA-designere, prosjektledere, tekniske ledere, forskere, siste års studenter og de største leverandørene på ett sted for 2 dagers praktisk fokus på FPGA.**

**Det blir foredrag fra norske bedrifter om utviklingsmetodikk og praktisk erfaring, universitetene presenterer nye og spennende prosjekter, og leverandørene stiller med aktuelle tekniske innlegg med et minimum av markedsføring. På utstillingen vil du kunne vurdere teknologi, verktøy og tjenester fra de ledende aktørene i bransjen.**

**FPGA-forum byr i tillegg på en ypperlig anledning til å møtes og utveksle erfaring innenfor FPGA-miljøet i Norge - både i pausene og under det sosiale arrangementet på kvelden.**

**In English:**

FPGA-forum is a yearly event for the Norwegian FPGA community. FPGA-designers, project managers, technical managers, researchers, final year students and the major vendors gather for a two-day focus on FPGA.
There will be presentations from the Norwegian industry about methodology and practical experience, - the universities will present new and exciting projects, and the vendors will have technical presentations with a minimum of marketing. At the exhibition, you can evaluate tools and technology from the leading vendors.
FPGA-forum also provides an excellent opportunity to meet and exchange experience with the Norwegian FPGA-community – during the breaks – and during the official dinner party on Wednesday.

**Half a year delayed due to Covid 19, but now we are back 😊**

# Programme Wednesday, September 7, 2022 (See abstracts below)

(Flags show spoken language. . means English on request. Slide language is normally the same as the title. If in doubt check appendix.)

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| **09.00** | Registration and coffee | |
| Session 1 | **Track AB** | |
| **09.25** | **Opening** (by Jim Tørresen and Espen Tallaksen) | |
| **09.30** | **Keynote by Clive "Max" Maxfield,**<br>**FPGAs and Other Awesome Technologies for the 21st Century**<br>(Introduced by Arild Kjerstad) | |
| **10.30** | **Vendor presentations** (3 min. per exhibitor - in alphabetical order) | |
| **11:10** | **Coffee break (and exhibition)** | |
| Session 2 | **Track A**<br>Session chair: Magnus Sjãlander | **Track B**<br>Session chair: Eivind Vågslid Skjæveland |
| **11.40** | **RISC-V® on Intel® FPGA**<br>Nikolay Rognlien, Arrow | **FPGAs and Post-Quantum Cryptography**<br>Matti Tommiska, Xiphera |
| **12:10** | **How can complex FPGA projects benefit from register automation?**<br>Nomita Goswami, FirstEDA | **User Terminal Wideband Modem for Very High Throughput Satellites (VHTS)**<br>Bjarne Risløw, WideNorth |
| **12:40** | **Lunch and Exhibition** | |
| Session 3 | **Track A**<br>Session chair: Per Gunnar Kjeldsberg | **Track B**<br>Session chair: Helge Fanebust |
| **14:00** | **UVVMs nye regresjonsverktøy**<br>Marius Elvegård, Inventas | **Microchip Multicore RISC-V based PolarFire® SoC platform – Linux & RealTime capable**<br>Davis Esselius, Microchip |
| **14:30** | **Highly efficient signal capture infrastructure for waveform extraction on FPGAs**<br>Nicola Vianello, ARM / Politecnico di Torino | **Beyond LUT's, FF's and routing – a look at how new FPGA building blocks advances system performance and capability.**<br>Jan Anders Mathisen, AMD/Xilinx |
| **15:00** | **Utilizing FPGAs as a tool for research in computer architecture**<br>Amund Bergland Kvalsvik, NTNU | |
| **15:30** | **Exhibition and Coffee** | |
| Session 4 | **Track A**<br>Session chair: Rune Bæverud | **Track B**<br>Session chair: Jim Tørresen |
| **16:00** | **Network Programmability kit for Ultra96**<br>Vladimir Vassilev, Lightside Instruments | **Bachelorstudie i elektronikk ved Høgskolen på Vestlandet**<br>Svein Haustveit, HVL |
| **16:30** | **Functional Safety on FPGA**<br>Andre Firing, EmLogic | **Presentasjon av Masteroppgaver**<br>**(For FPGA-forums pris for beste Masteroppgave 2021)** |
| **17:00** | **Toolbox for Safety critical design in RTL**<br>John Aasen, KDA | |
| **17:30** | **End of today's presentations** | |
| **19.30** | Aperitif TBD, Royal Garden Hotel | |
| **20.00** | Dinner party, Royal Garden Hotel.<br>Including a not to be missed dinner entertainment containing light and sound – for the first time at FPGA-forum | |

# Programme Thursday, September 8, 2022 (See abstracts below)

(Flags show spoken language. . means English on request. Slide language is normally the same as the title. If in doubt check appendix.)

| Session 5 | **Track A**<br>Session chair: Arild Kjerstad | **Track B**<br>Session chair: Per Gunnar Kjeldsberg |
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| **09.00** | **Experiences with NanoXplore's space-grade SRAM-based NG-MEDIUM FPGA**<br>Bendik Husa, UiB | **Cycle-accurate signal trace analysis on FPGA accelerated CPU simulations**<br>Björn Gottschall, NTNU |
| **09:30** | **Open-source radiation-tolerant CAN controller**<br>Simon Voigt Nesbø, HVL | **High-end Software Defined Radio (SDR)**<br>Christophe Coutand, WideNorth |
| **10:00** | **Using Python for a high-quality reusable verification environment.**<br>Faïçal Chtourou, InnoFour | **Nexus Platform FPGA**<br>Adam Clarkson, Lattice |
| **10:30** | **Exhibition and Coffee** | |
| Session 6 | **Track A.**<br>Session chair: John Aasen | **Track B**<br>Session chair: Magnus Jahre |
| **11:00** | **FPGA emulation of a new USB peripheral for a microcontroller**<br>Johannes Wågen, Egil Rotevatn and Lloyd Clark, Microchip Technology | **Lessons learned from porting MIL-1553 testbenches from TCL to UVVM.**<br>Arild Velure, Inventas |
| **11:30** | **Common path to embedded SoC design certification against 61508/50126/26262 and others.**<br>Alvaro Eguinoa de San Román, SafeTwice | **Enhanced Randomisation and Functional Coverage**<br>Espen Tallaksen, EmLogic |
| **12:00** | **Lunch and Exhibition** | |
| Session 7 | **Track A**<br>Session chair: Arild Kjerstad | **Track B**<br>Session chair: Johan Alme |
| **13:15** | **Formal verification using open-source tools.**<br>Egil Fykse, Appear | **Placing an FPGA on a board. Guidelines for efficient design/verification between FPGA and PCB environments**<br>Willem Gruter, HDL Works |
| **13:45** | **Using FPGAs, Python, gRPC, and Azure DevOps to automate ASIC prototyping and testing**<br>Espen Stenersen, Novelda | **Demystifying security with Intel FPGAs : device & platform level**<br>Nikolay Rognlien, Arrow |
| **14:15** | **Coffee break** | |
| Session 8 | **Track AB: Closing Keynotes**<br>Session chair: Per Gunnar Kjeldsberg and Jim Tørresen | |
| **14:45** | **Closing Keynote: Arild Søraunet, Norbit**<br>Is "Made in Norway" modern again? | |
| **15:30** | **Closing Keynote: Svein Even Blakstad, GRIFF Aviation**<br>GRIFF, the journey from a small west coast fjord - out into the big world | |
| **16:15** | Closing words | |
| **16:20** | The end | |

## Keynotes:

- Opening keynote:
  Clive “Max” Maxfield, Maxfield High-Tech Consulting.
  ***‘FPGAs and Other Awesome Technologies for the 21st Century’***
  *One of the great things about being Max is that -- since he writes about high-tech topics for various online publications, coupled with his providing technical writing and consulting services to a cornucopia of high-tech companies -- he gets to hear about many of the latest and greatest technologies before they appear on the market.*
  *Even better, Max is not tied to any subject sector or technological territory; instead, he’s free to meander around gathering noteworthy nuggets of knowledge and tasty tidbits of trivia. He may start the day learning about a new artificial intelligence neural network processor, after which he might find himself up to his armpits in virtual reality, and just a little later he could be feasting his eyes on next-generation camera-sensor combos that are only 1 mm thick for use in state-of-the-art machine vision systems -- and all of this before he’s had his breakfast.*
  *In this keynote presentation, in addition to the latest and greatest in FPGA space, Max says we will take a tour around a curated selection of the weird and wonderful things he’s been exposed to recently, focusing on anything that has made him exclaim, “Ooh, Shiny!” Max also notes that, as is usually the case in his presentations, we will be leaping from topic to topic with the agility of young mountain goats, so he urges attendees to dress appropriately and responsibly.*

- Closing keynote Day 2:
  Svein Even Blakstad, GRIFF Aviation
  ***‘GRIFF, the journey from a small west coast fjord - out into the big world’***
- Closing keynote Day 2:
  Arild Søraunet, Norbit
  ***'Is "Made in Norway" modern again?’***

## Price award for Best FPGA related Master thesis in Norway:

FPGA-Forum’s price is given to the best FPGA related Master thesis in Norway.

The award committee:

- Dag Andreas Hals Samuelsen, University College of Southeast Norway (USN)
- Jim Tørresen, University of Oslo

The nominees in alphabetical order:

- Harald Haugen Johnsen:
  "Efficient and accurate detection of illuminated points using FPGA hardware acceleration"
  Supervisor: Per Gunnar Kjeldsberg
  Department of Electronic Systems, NTNU
- Mateo Vazquez Maceiras:
  "Accelerating LBM on a Tightly-Coupled Field Programmable Gate Array"
  Supervisor: Magnus Jahre
  Department of Computer Science, NTNU
- Sondre Tagestad:
  "Hardware acceleration of compact CNN models for semantic segmentation of hyperspectral satellite images"
  Supervisors: Milica Orlandic
  Department of Electronic Systems, NTNU

All nominees will present their Master thesis in session 4B on day 1.
The winner will be announced during the dinner party.

**List of exhibitors (for Wednesday and Thursday):**

- Arrow Norway 1 (Intel, Lattice, Microchip) www.arrow.com
- Arrow Norway 2 (Intel, Lattice, Microchip) www.arrow.com
- Avnet Silica (AMD/Xilinx) www.silica.no
- EmLogic www.emlogic.no
- FirstEDA www.firsteda.com
- HDL works www.hdlworks.com
- InnoFour (Siemens EDA) www.innofour.com
- Lightside Instruments www.lightside-instruments.com

**Entertainment (during the dinner party):**

A not to be missed dinner entertainment containing light and sound – for the first time at FPGA-forum

**FPGA-forum Program-committee:**

- Arild Kjerstad, Kongsberg
- Hans Jørgen Fosse, Hagal
- Jan Anders Mathisen, Silica/Xilinx
- Jim Tørresen, University of Oslo
- Per Gunnar Kjeldsberg, NTNU
- Espen Tallaksen, EmLogic

# Titles and Abstracts for presentations at FPGA-forum 2022

**(In company alphabetical order)**

**Note that written and oral presentations may be in English or Norwegian. Some presenters may also switch to English on Request**
**Presentations are thus marked 'Written' or 'Oral' and E (English), N (Norwegian) or EoR (English on Request)**

| Company & Presenter | Title & Abstract |
|---|---|
| Aldec | See FirstEDA |
| Xilinx | See Avnet Silica |
| Appear<br>Egil Fykse<br><br>*Written: E, Oral: E* | **Formal verification using open-source tools**<br>We will present our experience with open-source formal verification tools. Bugs can be hidden in corner cases of the design that are not explored by the testbench, and formal verification can help find these bugs. This is a useful tool both for verification of new modules and bug hunting after a module has failed in the field. Some practical examples will be presented, as well as limitations of the tools. |
| ARM / Politecnico di Torino<br>Nicola Vianello<br><br>*Written: E, Oral: E* | **Highly efficient signal capture infrastructure for waveform extraction on FPGAs**<br>With the increasing complexity of modern VLSI designs, verification is becoming one of the biggest challenges for large semiconductor companies. Since they need to get the design in the market within a reasonable timescale, and the system is too complex to cover all possible input combinations and state transitions, different verification methodologies have to be mixed in order to exploit different advantages and to cover the holes left by other methods. One of these, that is now becoming mandatory to try a huge number of input patterns in an acceptable time-to-market, is the FPGA prototyping. With this technology it is easily possible to achieve a throughput of two orders of magnitude higher than in simulation, with the disadvantage of a limited internal visibility. Goal of my MSc thesis and 6-months internship at Arm in the Sophia CPU Verification team was to develop a solution to enhance FPGA internal visibility. This solution is based on a chain of tools which starts taking a file containing a list of signals as input, and after the FPGA test execution, will generate VCD dump of the selected signals during the last time window. The toolchain make use of an in-house Python/C++ framework able to manage streams of "events" in a very efficient way, and on a proprietary IP as interface between the software and the design to test. |

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| Arrow (Intel FPGA)<br>Nikolay Rognlien<br>**Exhibitor**<br><br>*Written: E, Oral: EoR* | **Demystifying security with Intel FPGAs : device & platform level**<br>FPGA device security can be a complex and overwhelming area for system architects and FPGA designers, with many opting to skip even basic security measures in their products. It doesn't have to be and shouldn't be this way; with many examples of vulnerabilities in products, security has never been more important. Intel FPGAs have some new security features which aim to make implementing security much easier.<br>The presentation will cover areas such as:<br>• Security attributes and attack vectors<br>• Authentication<br>• Encryption/Decryption<br>• Vendor Authorised Boot<br>• Attestation<br>• Black Key Provisioning<br>• Crypto Services<br>The aim is to give a technical overview of each topic, why it is valuable to the audience and how to implement in Intel FPGAs |
| Arrow (Intel FPGA)<br>Nikolay Rognlien<br>**Exhibitor**<br><br>*Written: E, Oral: EoR* | **RISC-V® on Intel® FPGA**<br>The RISC processor architecture has a long history and since its very beginnings as the "Berkeley RISC" in 1981 it has gone through various architecture generations. In 2010 the first RISC-V® implementation came to live at UC Berkeley and meanwhile this has emerged quite significantly. Today, different variants of 32-/64-/128-bit architectures exist, and the specification continues to be developed. The list of members in the RISC-V® organization is quite long and there are a few silicon devices and development boards available from different sources now.<br>Intel® who is a Premium Member of the RISC-V® organization does have a RISC type soft processor called NIOS® II which is used in the Intel® FPGAs already for more than a decade. Although Nios® II is highly versatile and configurable, it uses its own proprietary instruction set and tools.<br>Now Intel® has emerged its soft processor portfolio and started to ship the new FPGA soft processors called Nios® V/m which has a RISC-V® RV32IA compatible architecture. This not only enables much higher performance compared to the Nios® II but also allows to utilize the huge RISC-V® infrastructure and eco-system.<br>During this session we will look at the architecture and configuration options of the Nios® V/m core compared to the Nios® II processor version. We will investigate the hardware/software development and debugging flows as well as the usable eco-system. |
| Arrow (Lattice)<br>Adam Clarkson, Lattice<br>**Exhibitor**<br><br>*Written: E, Oral: E* | **Nexus Platform FPGA**<br>New families of Low power FPGA's with four different family members. All made on the 28 nm FD-SOI process which gives lower power and higher reliability than competing FPGA. The FPGA's range from 11K to 96K Logic Cells and the families have different hard IP's likes: 10 Gbps MIPI CSI-2 DPHY, 5G PCIe Gen2, SGMII CDR, ADC, 10GE PCS, PCIe Gen3 and Security blocks with Crypto. Come and hear how this can benefit you and your company. |
| Arrow (Microchip)<br>Davis Esselius,<br>Microchip<br>**Exhibitor**<br><br>*Written: E, Oral: E* | **Microchip Multicore RISC-V based PolarFire® SoC platform – Linux & RealTime capable**<br>Learn about Microchip's new PolarFire® SoC FPGA family innovative architecture,<br>combining low power consumption, thermal efficiency with defense grade security for smart, connected systems<br>able to address edge processing requirements for Industrial Automation, Automotive & Medical applications.<br>It's the first system on chip (SoC) field-programmable gate array (FPGA) with a deterministic,<br>coherent RISC-V CPU cluster enabling Linux and real-time applications. |

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| AvnetSilica (AMD/Xilinx)<br>Jan Anders Mathisen<br>**Exhibitor**<br><br>*Written: E, Oral: EoR* | **Beyond LUT's, FF's and routing – a look at how new FPGA building blocks advances system performance and capability.**<br>Throughout the history of FPGA's LUT's and FF's have been the basic building blocks from which anything digital could be built. Over the years more specialized primitives have been introduced that improves on performance, device utilization and power. The Versal ACAP family continues this evolution by introducing (among many other features) improved routing and highspeed math support. The presentation will look at the NoC and AIE/AIE-ML architectural elements as well as the integration of RF and HBM memory. |
| EmLogic<br>Andre Firing<br>**Exhibitor**<br><br>*Written: E, Oral: EoR* | **Functional Safety on FPGA**<br>Digital systems have become vital in controlling and monitoring safety critical systems where a failure can result in catastrophic consequences. With predictable behavior and fast response time, FPGAs are well suited for these applications. However, making safety critical designs brings on a new set of challenges for the FPGA designer. |
| EmLogic<br>Espen Tallaksen<br>**Exhibitor**<br><br>*Written: E, Oral: EoR* | **Enhanced Randomisation and Functional Coverage**<br>UVVM released brand new functionality on Enhanced Randomisation and Functional Coverage in October last year. As always with UVVM, testbench readability, overview and user friendliness where it matters the most, are the highest priorities.<br>This presentation will show you why and how, - and you will even get a mini course on Functional Coverage. |
| FirstEDA<br>Nomita Goswami<br>**Exhibitor**<br><br>*Written: E, Oral: E* | **How can complex FPGA projects benefit from register automation?**<br>As design complexity continues to increase, so does the number of registers residing on the HW/SW interface used to control the operations of the SoC/IP. The associated register definitions constantly evolve during the design cycle. A single register specification source means the required outputs can be automatically generated for the different teams.<br>In this presentation we will introduce SystemRDL 2.0 and discuss why this register description language is a preferred method of describing SoC/IP registers. We will cover register specification capture and describe an automated path from the specification to supporting documentation, HDL creation and other files that support the software access to the APIs. We will also explore the ability to parametrise components further, to improve design re-use and talk about the benefits of automation. |
| GRIFF Aviation<br>Svein Even Blakstad<br><br>*Written: E, Oral: EoR* | ***** Closing Keynote *****<br>**GRIFF, the journey from a small west coast fjord - out into the big world**<br>GRIFF Aviation is a Norwegian drone development company located in Sykkylven in Møre og Romsdal. They develop drones with a lifting capacity of 100 kg+. In this lecture, development manager Svein Even Blakstad takes us on the journey that the company has been through and the way forward into the future. There will be a focus on milestones achieved, challenges along the way and how they have been resolved. |
| HDL Works<br>Willem Gruter<br>**Exhibitor**<br><br>*Written: E, Oral: E* | **Placing an FPGA on a board. Guidelines for efficient design/verification between FPGA and PCB environments**<br>Developing hardware that involves an FPGA requires work in both an FPGA and a PCB design environment. They are separated environments but require close interaction. In this interaction there are different approaches and strategies possible. In my presentation I will outline guidelines, peculiarities of FPGA/PCB systems, useful naming conventions and explain why keeping a strict relationship between names on the FPGA and PCB will save you time and improve the quality of design. |

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| HVL<br>Simon Voigt Nesbø<br><br>*Written: E, Oral: E* | **Open-source radiation-tolerant CAN controller**<br>The Controller Area Network (CAN) bus protocol defines a fault-tolerant multi-master serial protocol. Originally it was intended for use in vehicles, but the robustness of the CAN protocol has made it a popular choice in a wide range of control applications, also in the radiation environments seen in space applications or high-energy physics experiments. Electronics designed for radiation environments often feature an FPGA, and employ Triple Modular Redundancy (TMR) to achieve radiation tolerance. There are several varieties of TMR, and the best choice is highly technology-dependent. We are presenting a new open-source CAN controller written in VHDL for FPGAs. The controller is highly configurable, but when used in a radiation environment, it features TMR techniques specifically tailored for SRAM FPGAs. |
| HVL<br>Svein Haustveit<br><br>*Written: N, Oral: N* | **Bachelorstudie i elektronikk ved Høgskolen på Vestlandet**<br>Litt om innhold i studiet med fokus på digitalteknikk, VHDL og FPGA.<br>Det har vært store endringer i fagområdet de siste 30 år.<br>Er det gamle tema som skal ut og nye som skal inn i undervisningen? |
| InnoFour | See Siemens EDA |
| Intel FPGA | See Arrow |
| Inventas<br>Arild Velure<br><br>*Written: E, Oral: EoR* | **Lessons learned from porting MIL-1553 testbenches from TCL to UVVM**<br>Legacy code tends to build up over time, so occasionally it is of benefit to sacrifice a bit of time to bring things up to date. In this presentation, we will go through the process we used for converting TCL testbenches to VHDL UVVM VIP, obstacles that were faced, and the benefits reaped at the end. The highlights are an increase in simulation speed, simpler integration with UVVM specification coverage and compatibility with GHDL, enabling us to run several regression simulations in parallel in CI without any incurred license cost.. |
| Inventas<br>Marius Elvegård<br><br>*Written: N, Oral: N* | **UVVMs nye regresjonsverktøy**<br>Et FPGA-design vil ofte ha et stort sett med tester som må kjøres for å verifisere funksjonaliteten. Et godt verktøy for effektiv og strukturert testing er derfor viktig. UVVM har nå fått et nytt regresjonsverktøy som er utviklet nettopp med tanke på dette; å effektivt kjøre konfigurerbare tester og å bygge en test-struktur hvor alle kjøreresultater er lett tilgjengelige. |
| KDA<br>John Aasen<br><br>*Written: E, Oral: E* | **Toolbox for Safety critical design in RTL**<br>In a safety critical design one should assume that everything can go wrong. Some error mitigations are done on the PCA level, and some are better suited for FPGAs. This presentation covers some concrete examples of how error mitigations can be implemented in safety critical systems. |
| Lattice | **See Arrow** |
| Lightside Instruments<br>Vladimir Vassilev<br>**Exhibitor**<br><br>*Written: E, Oral: E* | **Network Programmability kit for Ultra96**<br>We needed a platform similar to NetFPGA but for newer Zynq Ultrascale+ families. With free development tools license for Vivado. With an option to connect GNSS disciplined timing source. We also wanted it to be robust and preferably in a 1U rack form factor. We also wanted it to be modular within the 1U dimension limits. And we wanted the management software for the cores to be 100% based on YANG/NETCONF. And the YANG model to be a published open standard. And we wanted the toolchain for this software to be part of Debian. We also wanted a well known application to demonstrate this platform. We implemented a RFC2544 benchmark in python using the YANG/NETCONF interface. We produced all the prototypes at Bitraf (Oslo). We made the hardware and software open-source. |

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| Maxfield High-Tech Consulting<br>Clive "Max" Maxfield<br><br>*Written: E, Oral: E* | ***** Opening Keynote *****<br><br>**FPGAs and Other Awesome Technologies for the 21st Century**<br>One of the great things about being Max is that -- since he writes about high-tech topics for various online publications, coupled with his providing technical writing and consulting services to a cornucopia of high-tech companies -- he gets to hear about many of the latest and greatest technologies before they appear on the market.<br>Even better, Max is not tied to any subject sector or technological territory; instead, he's free to meander around gathering noteworthy nuggets of knowledge and tasty tidbits of trivia. He may start the day learning about a new artificial intelligence neural network processor, after which he might find himself up to his armpits in virtual reality, and just a little later he could be feasting his eyes on next-generation camera-sensor combos that are only 1 mm thick for use in state-of-the-art machine vision systems -- and all of this before he's had his breakfast.<br>In this keynote presentation, in addition to the latest and greatest in FPGA space, Max says we will take a tour around a curated selection of the weird and wonderful things he's been exposed to recently, focusing on anything that has made him exclaim, "Ooh, Shiny!" Max also notes that, as is usually the case in his presentations, we will be leaping from topic to topic with the agility of young mountain goats, so he urges attendees to dress appropriately and responsibly. |
| Microchip (FPGA) | **See Arrow** |
| Microchip Technology<br>Johannes Wågen, Egil Rotevatn and Lloyd Clark<br><br>*Written: E, Oral: E* | **FPGA emulation of a new USB peripheral for a microcontroller**<br>Designing and validating a new USB peripheral for a microcontroller is challenging. The complexity of the USB protocol makes verification difficult. Simulations take a long time to run and require a USB host that is simulated accurately. In order to speed up and improve the quality of the validation process, a complete microcontroller including the new USB peripheral was emulated on an FPGA. This allowed us to validate the hardware design with software stacks when connected to real USB hosts on all major operating systems. It also allowed errors to be injected at a far higher rate than simulations allow and confirm that the design is robust.<br>A standard Microchip debug and programming interface was included as part of the emulated microcontroller. This made it possible to use our standard software development tools such as Microchip Studio, and our Applications engineers could seamlessly perform software development and debugging just as if they had the finished production microcontroller in front of them. Software and hardware development could proceed in parallel, greatly tightening the schedule and allowing bugs to be found and fixed earlier.<br>This presentation outlines the choices we made and the experiences we had throughout this project, as well as lessons learned that may be valuable to anyone using FPGA emulation to reduce the risk of hardware design. |
| Norbit<br>Arild Søraunet<br><br>*Written: E, Oral: EoR* | ***** Closing Keynote *****<br>**Is "Made in Norway" modern again?**<br>NORBIT has gone against the flow and invested in both development and production in Norway. CTO of NORBIT, Arild Søraunet will talk about NORBIT's strategic investment and why they believe this is an investment for the future, seasoned with examples of exciting projects for Norwegian companies. |
| Novelda<br>Espen Stenersen<br><br>*Written: E, Oral: EoR* | **Using FPGAs, Python, gRPC, and Azure DevOps to automate ASIC prototyping and testing**<br>This presentation will talk about how Novelda is using an SoC FPGA board to test, validate, and characterize our Ultra-Wideband radar ASICs, using Python and gRPC to communicate with the board, and Azure DevOps to automate builds, testing and reporting. This platform enables an engineer to work connected or remote, and relaxes the computing and real-time requirements of a host communicating with a Novelda ASIC or prototyping FPGA. |

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| NTNU<br>Björn Gottschall<br><br>*Written: E, Oral: E* | **Cycle-accurate signal trace analysis on FPGA accelerated CPU simulations**<br>We have developed a profiling framework which allows us to efficiently analyze signal traces inside a cycle-accurate FPGA accelerated hardware simulation. We use it to measure application performance during the execution of industry standard benchmarks in a full-stack Linux system on a high performance out-of-order RISC-V CPU. For the first time, we were able to measure the execution latency of all instructions within a processor down to the single cycle. Using this data we created a golden performance reference which tells exactly how much time each instruction, function and application has spent executing. |
| NTNU<br>Amund Bergland Kvalsvik<br><br>*Written: E, Oral: E* | **Utilizing FPGAs as a tool for research in computer architecture**<br>Modern computer architecture research relies greatly on simulators, which seek to emulate the interactions occurring in real, physical processors. However, simulators obfuscate or fuzz many of the challenges real processor design faces, such as timing requirements, physical size, and coherent execution. Thanks to FPGAs, it is possible to perform real prototyping of design proposals, to improve transparency, insights, and transferability to industry. The presentation aims to introduce the benefits and limitations of using FPGAs a core part of your research, with examples from a completed master thesis. |
| SafeTwice<br>Alvaro Eguinoa de San Román<br><br>*Written: E, Oral: E* | **Common path to embedded SoC design certification against 61508/50126/26262 and others.**<br>The certification of safety-related devices, especially in high integrity cases, is a job that starts from conception. Nevertheless, in order to cover the requirements of the different standards, people can find themselves lost in a maze.<br>A key point is to follow a development path that encompasses both the product design and development as well as the certification. Using a complex 2002 architecture based on two Zinq 7000 devices with dual core cortex A9 embedded as an example, and detailing how technical issues are managed, mapping the process to the right toolset will result in a more understandable certification process for a number of standards, lowering risk and investment.<br>This presentation is aimed to show that a strong development process and a reliable toolset are key assets to success. |
| Siemens EDA / InnoFour<br>Faïçal Chtourou<br>**Exhibitor**<br><br>*Written: E, Oral: E* | **Using Python for a high-quality reusable verification environment.**<br>Constrained randomization and functional coverage have recently become crucial elements to a successful verification of FPGA and ASIC design. SystemVerilog and UVM framework is the de-facto standard for verification. Still, due to a high learning time/benefit ratio, many users preferred to look into other alternatives such as UVVM/OSVM.<br>Lately, Python has emerged as a third option, and it is gaining interest for its obvious advantages (easy language, big community, extensive library …)<br>The purpose of this presentation is to show you how we can build a high-quality reusable verification environment using Python Libraries/Framework. |
| UiB<br>Bendik Husa<br><br>*Written: E, Oral: E* | **Experiences with NanoXplore's space-grade SRAM-based NG-MEDIUM FPGA**<br>NG-MEDIUM is the first FPGA from the French company NanoXplore and it was made commercially available in 2018. This is a new and promising competitor in the range of available FPGAs for use in radiation-heavy environments. It is rad-hard by design, and produced in a rad-hard 65 nm CMOS process by STm. In addition, it features several mitigating techniques for radiation effects such as EDAC and a built-in and automatic configuration scrubber. It is the first European FPGA to be space qualified according to ESCC requirements in 2020, and as such the NanoXplore range is the only ITAR/EAR-free FPGA family of its kind.<br>I will walk you through both the architecture of the FPGA and the design flow using NanoXplore's Python-based software suite NanoXmap. I will also talk about my experiences working with this FPGA in a real design. |

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| WideNorth<br>Christophe Coutand<br><br>*Written: E, Oral: E* | **High-end Software Defined Radio (SDR)**<br>Presentation of the hardware design and the software framework for a powerful, modular SDR platform. |
| WideNorth<br>Bjarne Risløw<br><br>*Written: E, Oral: EoR* | **User Terminal Wideband Modem for Very High Throughput Satellites (VHTS)**<br>Presentation of a DVB-S2X Modem prototype supporting data rates up to 5 Gbps / 1.4 Gsps. |
| Xilinx | See Avnet Silica |
| Xiphera<br>Matti Tommiska<br><br>*Written: E, Oral: E* | **FPGAs and Post-Quantum Cryptography**<br>Large-scale quantum computers will outperform classical computers in solving certain hard computational problems.<br>Amongst these are RSA and elliptic curve discrete logarithm problem, which form the basis of contemporary public key cryptography underlying all Internet security.<br>NIST (National Institute of Standards and Technology) is currently running a PQC (Post quantum cryptography) competition to standardize quantum-secure public key cryptosystems.<br>The reconfigurability of FPGAs will play an important role in PQC adoption, as it will allow simultaneous support for both classical and PQC public key cryptography.<br>Another distinct advantage of FPGAs is algorithm agility, which will enable continuous support for the most recent versions of the evolving PQC standards.<br>The presentation will review the state-of-play of PQC standardization, and summarizes the current status of FPGA support for PQC algorithms. |