FPGA
forum

FPGA-forum 2016

The 11th FPGA-forum – where the Norwegian FPGA community meets

- FPGA-forum and exhibition: Wednesday 10 and Thursday 11 February 2016
- Tutorials/Workshops: Tuesday 9 February 2016

Britannia Hotel (Trondheim)

FPGA-forum er den årlige møteplassen for FPGA-miljøet i Norge. Her samles FPGA-designere, prosjektledere, tekniske ledere, forskere, siste års studenter og de største leverandørene på ett sted for 2 dagers praktisk fokus på FPGA.

Det blir foredrag fra norske bedrifter om utviklingsmetodikk og praktisk erfaring, universitetene presenterer nye og spennende prosjekter, og leverandørene stiller med aktuelle tekniske innlegg med et minimum av markedsføring. På utstillingen vil du kunne vurdere teknologi og verktøy fra de ledende leverandørene i bransjen.

FPGA-forum byr i tillegg på en ypperlig anledning til å møtes og utveksle erfaring innenfor FPGA-miljøet i Norge - både i pausene og under det sosiale arrangementet på kvelden.

In English:

FPGA-forum is a yearly event for the Norwegian FPGA community. FPGA-designers, project managers, technical managers, researchers, final year students and the major vendors gather for a two-day focus on FPGA.

There will be presentations from the Norwegian industry about methodology and practical experience, - the universities will present new and exciting projects, and the vendors will have technical presentations with a minimum of marketing. At the exhibition, you can evaluate tools and technology from the leading vendors.

FPGA-forum also provides an excellent opportunity to meet and exchange experience with the Norwegian FPGA-community – during the breaks – and during the official dinner party on Wednesday.

Programme Wednesday, February 10, 2016 (See appendix for abstracts and presentation language)

09.00	Registration and coffee	
09.25	**Opening**	
Session 1	**Track AB -** Session chair: Jim Tørresen, UiO and Espen Tallaksen, Bitvis	
09.30	**Keynote by Steve Furber, ICL Professor of Computer Engineering, The University of Manchester** From ARMs to Brains	
10.30	**Vendor presentations** (3 min. per exhibitor - in alphabetical order)	
11:10	**Coffee break (and exhibition)**	
Session 2	**Track A** Session chair: Hans Jørgen Fosse, Mikrokrets	**Track B** Session chair: Knut Wold, NTNU
11:40	**Single source fpga registers definition and Unix-like register access via serial, jtag and ethernet interfaces** Arin Morten Kjempenes, Progbit	**What has patents to do with FPGAs?** Torstein Dybdahl, Acapo AS
12:10	**A structured approach for firmware test environments** Olav Torheim, Data Respons	**mm Wave radar saves lifes at railway crossings - Embedded RF development success story** Tryggve Mathiesen, Qamcom
12:40	**Lunch and Exhibition**	
Session 3	**Track A** Session chair: Arild Kjerstad, Kongsberg	**Track B** Session chair: Torstein Dybdahl, Acapo
14:00	**Extending High Level Synthesis (HLS) beyond module generation – FPGA development moves toward SW centric methodology** Jan Anders Mathisen, AvnetSilica (Xilinx)	**Clockgates: A story of ASIC prototyping at Nordic Semiconductor** Per Magnus Østhus, Nordic Semiconductor
14:30		**MCU and Radio SoC Prototyping Using FPGAs** Filip Dovland, Silicon Labs
15:00	**Exhibition and Coffee**	
Session 4	**Track A** Session chair: Jim Tørresen, UiO	Track B Session chair: Arild Kjerstad, Kongsberg
15:30	**Presentasjon av Masteroppgaver (For FPGA-forums pris for beste Masteroppgave 2015)**	**UVM Framework – an easy way to improve your verification job** Stefan Bauer, Mentor Graphics (InnoFour)
16:00		
16:30	**Move to common track**	
Session 5	**Track AB -** Session chair: Espen Tallaksen, Bitvis	
16:35	**Closing Keynote: Mona Skaret, Innovasjon Norge** Flinke eller sinke på innovasjon?	
17:15	**End of today's presentations**	
19.30	Aperitif in the 'Lobby Lounge' outside 'Speilsalen', Britannia Hotel	
20.00	Dinner party in 'Speilsalen', Britannia Hotell. Entertainment: Pirum (Student choir)	

Programme Thursday, February 11, 2016 (See appendix for abstracts and presentation language)

Session 6	**Track A.** Session chair: Hans Jørgen Fosse, Mikrokrets	**Track B** Session chair: Tryggve Mathiesen, Quamcom
9:00	**Prototyping of ARM Mali GPUs for HW validation and SW co development, challenges and methodology** Jon Erik Oterhals, ARM	**FPGA-design for rominstrumentering - Utvikling av ASIM-instrumentet** Kjetil Ullaland, UiB (Universitetet i Bergen)
9:30	**2x Core Performance, 10x Memory Bandwidth – Really!** Nikolay Rognlien, Arrow (Altera)	**Design, Qualification and Production of space grade FPGA** Espen Flo Eriksen, Kongsberg Norspace
10:00	**Efficient Analysis of Large, Sparse Graphs on FPGAs** Yaman Umuroglu, NTNU	**Corner cases in Digital Design** Espen Tallaksen, Bitvis
10.30	**Exhibition and Coffee**	
Session 7	**Track A.** Session chair: Arild Kjerstad, Kongsberg	Track B Session chair: Hans Jørgen Fosse, Mikrokrets
11:00	**Quartus II Is Dead - Long Live Quartus Prime** Nikolay Rognlien, Arrow (Altera)	**Implementering av avansert modellprediktiv kontrollalgoritme til vekselretter som ei lavkostløysing i Xilinx ZynQ** Bjarte Hoff, UiT – Norges arktiske universitet
11:30	**Requirement driven development for safety-critical applications** David Clift, FirstEDA (Aldec)	**Securing M2M communications in an IoT system** Peter Trott, Avnet Memec
12:00	**Porting an ASIC node controller design to FPGA; Design and implementation challenges** Steffen Persvold, Numascale	
12:30	**Lunch and Exhibition**	
Session 8	**Track A** Session chair: Donn Morrison, NTNU	**Track B** Session chair: John Aasen, Kongsberg
13:45	**Motor control on a system-on-chip** Anders H. Bjørkto & Simen A. Tinderholt NTNU Revolve	**How to improve quality?** Dagrun Røyrvik , Cisco Systems Norway
14:15	**Design and Implementation of HD Vision Systems on FPGAs** Jonas Rutström, Mathworks	**Verifying corner cases in a structured manner - using VHDL Verification Components (VVC)** Espen Tallaksen, Bitvis
14:45	**Coffee break - and hand in evaluation forms**	
Session 9	**Track AB:** Session chair: Jim Tørresen UiO	
15:00	**Closing Keynote: Svein-Erik Hamran, Norwegian Defence Research Est./ University of Oslo** RIMFAX, a radar for the next NASA rover Mars 2020	
15:40	**Closing Keynote: Steinar Bjørnstad, CTO / Founder / Board Member of TransPacket** From idea searching for applications to market demand	
16:20	Closing words	
16:25	The end	

Keynotes:

- Opening keynote: Steve Furber, ICL Professor of Computer Engineering, The University of Manchester
  From ARMs to Brains
- Closing keynote D1: Mona Skaret, Innovasjon Norge
  Flinke eller sinke på innovasjon?
- Closing keynote D2: Steinar Bjørnstad, CTO / Founder / Board Member of TransPacket
  From idea searching for applications to market demand
- Closing keynote D2: Svein-Erik Hamran, Norwegian Defence Research Est./ University of Oslo
  RIMFAX, a radar for the next NASA rover Mars 2020

See more info on the keynotes in the appendix.

Price award for Best FPGA related Master thesis in Norway:

FPGA-Forum's price is given to the best FPGA related Master thesis in Norway.

The award committee:

- Knut Wold, Høgskolen i Gjøvik (Gjøvik University College)
- Kjetil Ullaland, Universitetet i Bergen (University of Bergen)
- Hans Jørgen Fosse, Mikrokrets

The nominees in alphabetical order:

- Andreas Bertheussen, - Department of Electronics and Telecommunications, NTNU
  Supervisor: Bjørn B. Larsen
  Adaptive Beamforming Using the Recursive Least Squares Algorithm on an FPGA

- Benjamin Bjørnseth, Department of Computer and Information Science, NTNU
  Supervisor: Lasse Natvig
  Enabling Research on Energy-Efficient System Software Using the SHMAC Infrastructure

- Jadaan Diaa, - Department of Engineering Cybernetics, NTNU
  Supervisor: Amund Skavhaug
  FPGA Based Real-time Systems Tester

All nominees will present their Master thesis in the last session on day 1.
The winner will be announced during the dinner party.

Workshops:

There will be one workshop on day 0 of FPGA-forum, - Tuesday 9 February

- MathWorks:
  FPGA and SoC Design using MATLAB and Simulink
  For information and registration see:
  https://go2.mathworks.com/fpga-and-soc-design-using-matlab-and-simulink-sem-se-1247556?ul=en&uc=SE

List of exhibitors (for Wedn. 10 and Thur. 11 February):

• ARM Norway	www.arm.com
• Arrow Norway (Altera)	www.arrowne.com
• Avnet Memec (Microsemi/Actel)	www.microsemi.com
• Avnet Silica (Xilinx)	www.silica.no
• Bitvis	www.bitvis.no
• Embida	www.embida.no
• FirstEDA (Aldec, OneSpin, Sigasi, SynthWorks)	www.firsteda.com
• Innofour (Mentor)	www.innofour.com
• MathWorks	www.mathworks.com
• ProgBit	www.progbit.no
• Qamcom	www.qamcom.se
• Synective	www.synective.se

Entertainment (during the dinner party):

Pirum (Student choir)

FPGA-forum Program-committee:

- Arild Kjerstad, Kongsberg
- Hans Jørgen Fosse, Mikrokrets
- Jan Anders Mathisen, Silica/Xilinx
- Jim Tørresen, Universitetet i Oslo
- Espen Tallaksen, Bitvis

Titles and Abstracts for presentations at FPGA-forum 2016

(In company alphabetical order)

Note that written and oral presentations may be in English or Norwegian. Some presenters may also switch to English on Request
Presentations are thus marked 'Written' or 'Oral' and E (English), N (Norwegian) or EoR (English on Request)

Company & Presenter	Title & Abstract
Acapo AS Torstein Dybdahl *Written: E, Oral: E*	**What has patents to do with FPGAs?** How and what can be patented in FPGA implementations? When does patents have value? When should I fear other granted patents? Real life examples of why and where FPGA related patents give value.
Aldec	See FirstEDA
Altera	See Arrow
ARM Jon Erik Oterhals *Written: E, Oral: E*	**Prototyping of ARM Mali GPUs for HW validation and SW co development, challenges and methodology** The ARM Mali GPUs originally developed by the Trondheim based start-up company Falanx Microsystems which ARM acquired in 2006 can now be found in flagship devices like the Samsung Galaxy S6. Part of this success history can be contributed to the effective use of FPGA technology for HW validation and SW co development. The GPUs under development are continuously ported to FPGAs in various configurations and large farms of FPGA platforms are used in automated HW and SW regressions. This enables both running trillions of cycles for HW validation daily, and also do nightly SW regressions runs on new GPU's enabling us to deliver conformant SW drivers even before any silicon has been produced. This presentation will focus on how we have built a fully automated FPGA image build process and what kind of challenges we have faced and are still facing in doing so. Also it's not just about running lots of cycles on FPGAs, but you would also need to have a way to debug any failures observed. To aid the debug we have developed an in house debug methodology which enables us to get 100% visibility of any signals inside the GPU for almost unlimited cycle counts.
Arrow (Altera) Nikolay Rognlien *Written: E, Oral: EoR*	**2x Core Performance, 10x Memory Bandwidth – Really!** Altera has announced a number of technology firsts with its high-end Stratix 10 FPGA family. Join Nikolay Rognlien of Arrow Electronics as he explains how Altera's HyperFlex FPGA architecture can enable 1GHz core FPGA system clocks and how using Intel System-in-Package (SiP) technology Altera is able to integrate massive 3D stacked High-Bandwidth Memory (HBM) that elevates traditional restrictive memory interfaces. These capabilities are firsts for the Stratix 10, but they'll be coming to mid-range FPGAs soon.
Arrow (Altera) Nikolay Rognlien *Written: E, Oral: EoR*	**Quartus II Is Dead - Long Live Quartus Prime** Altera has updated and rebranded its development software. Join Nikolay Rognlien of Arrow Electronics as he introduces Altera's third high level synthesis compiler A++, how it integrates into Quartus and differs from other such tools, and the overall productivity gains delivered by Quartus Prime.

Avnet Memec (MicroSemi) Peter Trott *Written: E, Oral: E*	**Securing M2M communications in an IoT system** In the public network (Internet), digital certificates or public key certificates are often used to secure communication links. A public key certificate is an electronic document that contains both an identity and a public key, binding them together by a digital signature. The public key certificates are an important part of transport layer security (TLS), where they prevent an attacker from impersonating as a trusted client or server, commonly called a man in the middle attack. The most common certificate format is defined by the X.509 standard. In a PKI, the process of submitting a certificate request is known as enrolment. After enrolment, the Certificate Authority, issues a public key certificate to the enrolled public key. During the enrolment, the device that submits the public key is required to prove that it knows the associated private key and that it controls the use of this private key. Elliptic curve cryptography (ECC) is emerging as an attractive public-key cryptosystem, in particular for mobile (that is, wireless) environments. Compared to currently prevalent cryptosystems such as RSA, ECC offers equivalent security with smaller key sizes. Smaller key sizes result in savings for power, memory, bandwidth, and computational cost that makes ECC especially attractive for constrained environments. The premium S grade SmartFusion2 devices (M2S060S, M2S090S, and M2S150S) have a built-in ECC hardware accelerator (that is, NIST-defined P-384 curve) to support public-key cryptographic techniques for key establishment. This paper demonstrates the ability of the SmartFusion2 SoC FPGA device to self-enrol in PKI and obtain a digital certificate to securely exchange messages with another device in the PKI to meet the security challenges of wireless M2M communications in an IoT system.
AvnetSilica (Xilinx) Jan Anders Mathisen *Written: E, Oral: N*	**Extending High Level Synthesis (HLS) beyond module generation – FPGA development moves toward SW centric methodology** Numerous applications (HPC, test & measurement) may benefit from FPGA-technology to accelerate critical functionality. The challenge is that developers are predominantly SW engineers with little experience in HW design or SW/HW interfacing. Recent developments in raising abstraction levels beyond RTL through the use of High Levels Synthesis (HLS) are trying to bridge the gap between SW and HW – but have still remained rather HW centric. This presentation will look at how abstraction levels can be further raised to allow SW developers and end users to comfortably explore the use of FPGA technology without leaving the familiar SW development domain – moving toward SW centric development methodology for FPGA systems.
Bitvis Espen Tallaksen *Written: E, Oral: E*	**Corner cases in Digital Design** All FPGA (And ASIC) design have lots of corner cases in their specification and implementation. These corner cases very often lead to design errors due to the simple fact that they are inherently error prone and difficult to detect and check. This presentation will show some typical examples of different types of corner cases – and also discuss how we can reduce the amount of corner cases and check that the remaining corner cases behave correctly. (This presentation applies to FPGAs and ASICs alike, and is HDL language independent.)

Bitvis Espen Tallaksen *Written: E, Oral: E*	**Verifying corner cases in a structured manner - using VHDL Verification Components (VVC)** Most testbenches do not properly verify corner cases in a DUT (Device Under Test, e.g. FPGA or an FPGA module). And most attempts to do so lead to chaotic testbench code and a very time consuming verification phase. UVVM (Universal VHDL Verification Methodology) was released in 2015 to solve this problem. Bitvis Utility Library (open source released 2013), which is currently being used in lots of companies in Norway and internationally is now a part UVVM. This library provides procedures and functions that are very simple to use, but makes testbench implementation a lot easier and faster – even for novice designer, - resulting in time saved, better quality, better overview and significantly improved maintainability. In 2015 UVVM VVC Framework was released. This is a verification component system that allows the implementation of a very structured testbench architecture to handle medium complexity verification challenges and upwards. The key benefit of this system however, is the fact that a very simple software-like VHDL test sequencer may now easily control the complete testbench architecture with all the verification components. This takes overview, readability and maintainability to a new level. Some corner cases are easily covered by applying constrained random stimuli, but covering cycle related corner cases requires a more structured approach – as multiple interfaces of a DUT must be controlled simultaneously. The VVC Framework provides a major step improvement in handling such challenges. Going from just a set of BFM (Bus Functional Model) procedures to a complete verification component for that interface, is a really fast operation thanks to the structure and script support. For a UART it took less than an hour – even before the script support. This presentation will show how the UVVM VVC Framework can be used to verify corner cases in a DUT, and also show the simplicity of the VHDL test sequencer and how debugging can be made far more efficient.
Cisco Systems Norway Dagrun Røyrvik *Written: E, Oral: EoR*	**How to improve quality?** This is the question the FPGA team got from the management in Cisco last autumn. The other teams got the same question. The simple answer could have been: Quality is already good at FPGA. But as our SVP says – Good is average, and average is irrelevant. So we chose to focus on quality for a limited period of time. Important project tasks were put on hold, and we spent time on tools and processes for automation of work flow. The presentation will cover our work flow in general and the improvements done in particular. What did we do? What did we gain? Did quality improve? Was it worth it?
Data Respons Olav Torheim	**A structured approach for firmware test environments** It is common knowledge that structured approaches are necessary for successfull firmware design. However, the same structured approach is normally omitted when building the test benches for the same firmware designs. Instead, simple and sequential tests are performed in the simulation testbench, with the more complicated scenarios tested out directly in hardware. Such approaches lead to a lot of corner cases which are never discovered in simulation, and maybe not even in the hardware test – resulting in malfunctioning applications at the customer. Data Respons Firmware Development Kit is a structured methodology for construction test benches. It also has a rich library of verification units, allowing verification at both bus functional level and system level. With this approach, executable firmware specifications can be developed and run in the simulation environment, providing also an excellent starting point for the following hardware test. The entire library is written in pure VHDL and comes with all source code available. No additional software tools are required. It is therefore an excellent alternative to expensive closed-source verification tools.

FirstEDA (Aldec) David Clift *Written: E, Oral: E*	**Requirement driven development for safety-critical applications** The verification of a safety critical product starts with the requirements, so it is critical that they are correct, complete, unambiguous, verifiable and logically consistent. The problem with requirements is that they are subject to change and are often poorly defined. Such problems and the ever-growing complexity of today's FPGAs necessitate management of the requirements throughout the development process and product life cycle. In this presentation we will look at a making requirements central to the design and verification process: Requirements-Based Verification (RBV). Such an approach addresses three key areas: • Ensures that requirements are correct & complete • Ensures that the design correctly implements the requirements • Ensures final product meets the requirements
InnoFour (Mentor Graphics) Stefan Bauer (Mentor Graphics) *Written: E, Oral: E*	**UVM Framework – an easy way to improve your verification job** Advanced verification methodologies like UVM (Universal Verification Methodology) enable higher level efficiency and re-usable structure. However many product teams do not take such productivity and quality benefits because they overestimate the ramp-up time required to introduce UVM. In order to increase the time-to-productivity Mentor Graphics created a framework. The so called UVM Framework provides a set of common UVM based testbench building blocks that are ready to use without the necessity of detailed UVM knowledge. In this session you will get a short overview of the UVM Framework followed by a live-demo.
Innovasjon Norge Mona Skaret *Written: ?, Oral: N*	***** CLOSING KEYNOTE Day 1: 'Flinke eller sinke på innovasjon?'** Sjelden har det vært viktigere å skape nye jobber og eksportbedrifter som utfordrer det etablerte med ny teknologi og nye måter å jobbe på. Men er vi fortsatt for forelsket i teknologien til å lykkes internasjonalt og bygge en sterk nasjonal merkevare? Hvorfor jobber ikke big corporates og små startups mer sammen? Kan vi bruke våre beste næringsklynger mer til å utvikle nye løsninger på tvers av fag og sektorer?
Kongsberg Norspace Espen Flo Eriksen *Written: E, Oral: N*	**Design, Qualification and Production of space grade FPGA** FPGA technology has become relatively common in space grade electronics hardware, and in many units it is one of the most functionally complex parts. It is therefore considered to be a critical component and FPGAs receive special attention throughout both the design and delivery phases. The presentation will address the specific topics encountered in a full space grade FPGA project starting with the specifications and design phase. Then moving on to the verification and qualification of the design and finally production, test and delivery of the flight hardware.
Mathworks Jonas Rutström *Written: E, Oral: E*	**Design and Implementation of HD Vision Systems on FPGAs** Frames to pixels and pixels to frames. Learn how to implement and verify HD vision processing algorithms on FPGAs using MathWorks tools. This presentation will focus on how to bridge the gap between algorithm designers and FPGA designers enabling an efficient workflow for successful design of vision systems. Highlights: • High level design • HDL code generation • Pixel-streaming algorithms for design and implementation • Early verification and FPGA-in-the-Loop simulation
Mentor Graphics	See Innofour
MicroSemi	See Avnet Memec

Nordic Semiconductor Per Magnus Østhus *Written: E, Oral: EoR*	**Clockgates: A story of ASIC prototyping at Nordic Semiconductor** Challenges and experiences using FPGA's for ASIC prototyping. Plus a look into how FPGA's can enable an Agile SoC development flow.
Norwegian Defence Research Est./University of Oslo Svein-Erik Hamran	***** CLOSING KEYNOTE Day 2: 'RIMFAX, a radar for the next NASA rover Mars 2020'** Radar Imager for Mars' Subsurface Experiment - RIMFAX is one of seven instruments selected for the NASA Mars 2020 rover mission. RIMFAX is a Ground Penetrating Radar transmitting electromagnetic waves from 150 Mhz to 1200 Mhz into the ground. The radar can potentially penetrate to more than 10 meter into the Martian subsurface and reveal the geological and environmental history of Mars. The presentation will give a short overview of the Mars 2020 mission and discuss the development of the RIMFAX radar system. Results from the first field test of a prototype model will be presented.
NTNU Yaman Umuroglu *Written: E, Oral: E*	**Efficient Analysis of Large, Sparse Graphs on FPGAs** Analysis of large, sparse graphs are imporant in a variety of domains including social network analysis, bioinformatics, electronic design automation, compressed sensing and economic modeling. Processing such graphs with high performance and energy efficiency requires hardware platforms that can effectively handle irregular parallelism and memory accesses. General-purpose CPUs and GPGPUs do not align well with these requirements and can typically utilize only a small fraction of their capabilities for these problems. New generation FPGAs with access to high bandwidth memory and partial dynamic reconfiguration have the potential to be the platform that big graph processing needs. In this presentation we will present our recent research on developing efficient FPGA accelerators for sparse graph algorithms.
NTNU (revolve project) Anders H. Bjørkto & Simen A. Tinderholt	**Motor control on a system-on-chip** 'Hovedpunktene vi skal innom er hvorfor motor(og inverter-) kontroll gjøres bedre på SoC enn mikrokontroller/FPGA. Innom forskjellige typer motorkontrollalgoritmer: FOC, FOC(SVPWM), DTC. Timing issues på microcontroller. Hvordan det gjøres på FPGA (microblaze -> "SoC" - veie opp mot hverandre. hvordan SoCs samler problemer i en løsning'
Numascale, Steffen Persvold *Written: E, Oral: EoR*	**Porting an ASIC node controller design to FPGA; Design and implementation challenges** Node controllers are necessary to interconnect CPU specific coherency fabrics in order to form large coherent shared memory computer systems. These systems have advantages compared to traditional single server systems with workloads in areas such as Big Data Analytics, Genomics and IoT. With our NumaChip 1 ASIC technology, we built the worlds largest single coherent shared memory computer with 108 nodes, more than 5000 cores and 20TByte of RAM. In this presentation we'll present the implementation of the next generation NumaChip 2 Node Controller chip on a FPGA platform, and the challenges encountered in the process.
Progbit Arin Morten Kjempenes *Written: E, Oral: E*	**Single source fpga registers definition and Unix-like register access via serial, jtag and ethernet interfaces** FPGA registers are defined and accessed in many different settings like simulation, prototyping and finished product. There are several vendors, tools and protocols to relate to. It is time consuming and error prone. The Autoreg and Autocom tools from ProgBit provides single source register definition and seamless access methods that covers simulation, sw, lab sw and test sw. It supports serial, JTAG and Ethernet (ip/udp) interfaces. It support both Altera and Xilinx. The registers are defined in a simple text format and vhdl, c and tcl code is auto-generated. The registers are accessed via simple get and set commands using register names and the hierarchy is traversed and searched via familiar Unix-like commands like cd, ls and find.

Qamcom Tryggve Mathiesen *Written: E, Oral: E*	**mm Wave radar saves lifes at railway crossings - Embedded RF development success story** Automobile accidents are currently killing 1.25 million people per year worldwide and soon it will reach 2 million people per year. A chilling statistic. The new mantra is “avoiding collisions.” Qamcom 77 GHz short range Radar - Obstacle Detector System – have been improving safety for unsupervised railway crossings, but the radar is scalable for collision avoidance on moving cars/trucks, and ongoing development will make the platform capable to be used as sensor system for autonomous vehicles, upgraded to 79 GHz. The successful 77 GHz radar uses FPGA for high speed A/D sample preprocessing, cooperation with a powerful SOC with DSP functionality. The FPGA solution is very capable for the preprocessing and SRIO protocol conversion, but with the 79 GHz enhancement the sample rate will multiply 10 times. The 79 Ghz radar will need to move the signal processing algorithms and radar control towards the FPGA domain, and the scalable SW Defined development environment for FPGAs offers a software-centric, system-optimizing compiler that accepts existing system-level design in C or C++ and generates both the software application and the hardware configuration needed to implement the enhanced system. The new FPGA tools employs software compilers, HLS (high-level synthesis), and prebuilt hardware infrastructure to assemble such systems.
Silicon Labs Filip Dovland *Written: E, Oral: E*	**MCU and Radio SoC Prototyping Using FPGAs** At Silicon Labs we use FPGAs as an integral part of our pre-tapeout verification process for MCUs and radio SoCs. In this talk I will describe how we have built an FPGA solution that integrates seamlessly with our existing tools and infrastructure, how this supports our digital design verification, regression suite and SW development, and how we are able to verify radio IP using channel emulation over Ethernet.
TransPacket Steinar Bjørnstad *Written: E, Oral: E*	***** CLOSING KEYNOTE Day 2: 'From idea searching for applications to market demand'** It can be a long way from a basic technology research idea to a product. For such technologies, there may be several business areas where it may show to be useful. Integrated Hybrid Optical Networks (IHON) fully integrates circuit and packet switching into the same link-resource. TransPacket has commercialized the technology into a product currently being deployed in fibre optical carrier telecom networks. However, because of the technologies basic deterministic timing properties it proves out to be useful in a number of applications ranging from control in industrial production lines to cars. The idea is no longer looking for an application, the market demands the technology.
UiB (Universitetet i Bergen) Kjetil Ullaland	**FPGA-design for rominstrumentering - Utvikling av ASIM-instrumentet** Institutt for Fysikk og Teknologi ved Universitetet i Bergen har utviklet to detektorer som skal brukes til studier av gammaglimt fra tordensystemer, såkalte Terrestrial Gamma Flashes (TGF). Detektorene er en del av MXGS-instrumentet som inngår i ASIM (Atmosphere-Space Interactions Monitor), som skal installeres på den internasjonale romstasjonen i 2017. Detektor-utlesningssystemet består av ASIC’er for utlesning av 16384 solid-state detektorpiksler (for røntgen og lave gamma-energier), og diskret elektronikk for utlesning av 12 fotomultiplikatorrør koblet til scintillasjonskrystaller (for høye gamma-energier). Datainnsamlingen og signalprosesseringen er FPGA-basert. Siden instrumentet skal brukes i rommet er det strenge krav til pålitelighet og strålingstoleranse, og derfor er RTAX2000 fra Microsemi (Actel) valgt. RTAX-serien er en strålingsherdet anti-fuse teknologi, som betyr at FPGA’en må programmeres før den loddes på kretskortet. Dette stiller strenge krav til verifikasjon og testing i og med at oppdatering av firmware etter montering ikke er mulig. Prototyping er derfor først gjort med flash-baserte kretser (ProAsic3E) og deretter anti-fuse kretser (AX2000) i sokkel. Foredraget vil omtale hardware- og firmware-designet med fokus på erfaringer relatert til rominstrumentering.

UiT – Norges arktiske universitet Bjarte Hoff *Written: E, Oral: E*	**Implementering av avansert modellprediktiv kontrollalgoritme til vekselretter som ei lavkostløysing i Xilinx ZynQ** Nye og avanserte modellprediktive kontrollalgoritmar innan kraftelektronikk er avhengig av svært høg ytelse, sidan mange utrekningar må utførast på kort tid. Samtidig må maskinvara vera rimelig, dersom det skal kunne ha kommersielle bruksområder. I dette prosjektet, har eit MicroZed utviklingskort med Xilinx Zynq SoC blitt brukt til å implementere ei slik løysing ved Sulkowski-laboratoriet på Høgskolen i Narvik. Kombinasjonen av mikroprosessor og programmerbar logikk, saman med integrerte analoge inngangar, har vist seg avgjerande for å utføra desse berekningane raskt nok som flyttalsoperasjonar på rimelig maskinvare. Prosjektet er blitt utvikla og testa på ein vekselrettar som emulera solcelleenergi levert til kraftnettet. Presentasjonen fokusera på oppbygging av arkitekturen og dei mulegheitene i ZynQ som har vert avgjerande under utviklinga. Det blir også vist kva ytelse dette har resultert i.
The University of Manchester Steve Furber *Written: E, Oral: E*	***** OPENING KEYNOTE: 'From ARMs to Brains'** Back in the early 1980s the BBC Microcomputer introduced a generation of UK schoolchildren to computer programming. The BBC Micro was developed by Acorn Computers Ltd, based in Cambridge, UK. Following the success of the BBC Micro, Acorn looked for a microprocessor around which to base its product evolution, but the standard industry offerings did not meet Acorn's requirements, so they embarked on the ambitious plan to develop their own processor. The result - the Acorn RISC Machine, or ARM - was small and simple, and turned out to be ideally suited to the emerging System-on-Chip market of the 1990s. Today descendants of the original ARM, now developed by ARM Ltd, dominate the mobile consumer market, and over 60 billion have been shipped by ARM's many semiconductor partners. The SpiNNaker (Spiking Neural Network Architecture) project at the University of Manchester, UK, is building a million ARM processors into a highly configurable platform for brain-modelling applications. The information processing principles at work in the brain remain as one of the great mysteries of science, and with SpiNNaker we hope to contribute to unlocking this mystery, in collaboration with many others through vehicles such as the EU ICT Flagship Human Brain Project.
Xilinx	See Avnet Silica