Last update Feb. 4

FPGA-forum 2015

The 10th FPGA-forum – where the Norwegian FPGA community meets

- FPGA-forum and exhibition: Wednesday 11th and Thursday 12th of February 2015

Britannia Hotel (Trondheim)

FPGA-forum er den årlige møteplassen for FPGA-miljøet i Norge. Her samles FPGA-designere, prosjektledere, tekniske ledere, forskere, siste års studenter og de største leverandørene på ett sted for 2 dagers praktisk fokus på FPGA.
Det blir foredrag fra norske bedrifter om utviklingsmetodikk og praktisk erfaring, universitetene presenterer nye og spennende prosjekter, og leverandørene stiller med aktuelle tekniske innlegg med et minimum av markedsføring. På utstillingen vil du kunne vurdere teknologi og verktøy fra de ledende leverandørene i bransjen.
FPGA-forum byr i tillegg på en ypperlig anledning til å møtes og utveksle erfaring innenfor FPGA-miljøet i Norge - både i pausene og under det sosiale arrangementet på kvelden.

In English:
FPGA-forum is a yearly event for the Norwegian FPGA community. FPGA-designers, project managers, technical managers, researchers, final year students and the major vendors gather for a two-day focus on FPGA.
There will be presentations from the Norwegian industry about methodology and practical experience, - the universities will present new and exciting projects, and the vendors will have technical presentations with a minimum of marketing. At the exhibition you can evaluate tools and technology from the leading vendors.
FPGA-forum also provides an excellent opportunity to meet and exchange experience with the Norwegian FPGA-community – in the breaks – and during the official dinner party on Wednesday.

Official website for FPGA-forum: www.fpga-forum.no

Hotel

A special discount price of NOK 1095 is available for conference participants at Hotel Britannia (Dronningens gate 5). For reservations either select this option ('Single room Britannia Hotel NOK 1 095,00') when registering for the event or call +47 73800800 and refer to Tekna's FPGA-forum.

Programme Wednesday, February 11, 2015 (Note: See appendix for abstracts)

09.00	Registration and coffee	
09.25	**Opening**	
Session 1	**Track AB -** Session chair: Espen Tallaksen, Bitvis	
09.30	**Keynote by Adam Taylor, Head of Engineering - High Performance Imaging Solution Division, e2v** 'What will ET make of My FPGA choice'	
10.30	**Vendor presentations** (3 min. per exhibitor - in alphabetical order)	
11:10	**Coffee break (and exhibition)**	
Session 2	**Track A** Session chair: John Aasen, Kongsberg	**Track B** Session chair: Kjetil Svarstad, NTNU
11:30	**Felles simuleringsmiljø gjør FPGA utviklerens hverdag enklere** Kristin Aksnes, KDA	**Synopsys HAPS Developer eXpress – Accelerated Transactors based IP prototyping case study** Antti Innamaa, Synopsys
12:00	**Register Wizard: Single source register information** Sverre Vigander, Bitvis	**FPGA and SoC Design from Idea to Implementation** Jonas Rutström, Mathworks
12:30	**Lunch and Exhibition**	
Session 3	**Track A** Session chair: Arild Kjerstad, Kongsberg	**Track B** Session chair: Per Gunnar Kjeldsberg, NTNU
13:45	**Automatic register generation with corresponding protocol and APIs for simulation, lab test and final product access** Arin Morten Kjempenes, Progbit	**Five Years Context Switching of FPGAs – Ready to Start Executing?** Jim Tørresen, Universitetet i Oslo
14:15	**Exact Probability of Undetected Error (Pude) for shortened linear error-detection block codes via brute-force calculation in FPGA logic** Anne Elisabeth Vallestad, ABB	**Powering FPGAs efficiently and easy.** Nikolay Rognlien, Arrow (Altera)
14:45	**Exhibition and Coffee**	
Session 4	**Track A** Session chair: Jim Tørresen, University of Oslo	Track B Session chair: Johan Alme, Bergen Univ. College
15:15	**Real examples of embedded design in Zynq** Jan Anders Mathisen, Avnet Silica (Xilinx)	**VUnit - A Unit Testing Framework for VHDL** Lars Asplund, Synective Labs
15:45		**When failure is not an option! Static Verification For FPGAs** David Clift, FirstEDA (Aldec/OneSpin)
16:15	**Move to common track**	
Session 5	**Track AB - Closing Keynote.** Session chair: Hans Jørgen Fosse, Mikrokrets	
16:20	**Closing Keynote: Pat Mead – FAE Manager, Altera Europe** How convergence is re-writing the FPGA industries development landscape.	
17:00	**End of today's presentations**	
18.30	Aperitif in the 'Lobby Lounge' outside 'Speilsalen', Britannia Hotel	
18:45	**Ut på tur med Stein P. Aasheim – en reise i bilder og livserfaringer** (more info in programme) (Travelling with Stein P. Aasheim – a journey through photos and life experience)	
20.00	Dinner party in 'Speilsalen', Britannia Hotell. Entertainment: Candiss (Student choir)	

Programme Thursday, February 12, 2015 (Note: See appendix for abstracts)

Session 6	**Track AB: Opening Keynote** Session chair: Arild Kjerstad, Kongsberg	
09.00	**Opening Keynote: Jim Lewis, VHDL Training Expert, SynthWorks** The Whys and Whats of Advanced Verification	
10.00	**Exhibition and Coffee**	
Session 7	**Track A.** Session chair: Roar Skogstrøm, Kongsberg	**Track B** Session chair: Hans Jørgen Fosse, Mikrokrets
10:45	**Going from Virtex-2 pro to SmartFusion2 – Learning by doing (Mistakes)** Johan Alme, Universitetet i Bergen	**Bridging the FPGA World and the PCB** Rick Stroot, InnoFour (Mentor Graphics)
11:15	**Stratix10 HyperFlex Architecture** Nikolay Rognlien, Arrow (Altera)	**Qualifying FPGAs for use in a Radiation Environment** Chengxin Zhao, Universitetet i Oslo
11:45	**UVVM: Universal VHDL Verification Methodology ("UVM for VHDL")** Espen Tallaksen, Bitvis	**SecureBoot-FPGA Anti-Tamper Solution** Peter Trott , Avnet Memec (MicroSemi)
12_15	**Lunch and Exhibition**	
Session 8	**Track A** Session chair: Anne Elisabeth Vallestad, ABB	**Track B** Session chair: Knut Wold, Gjøvik University College
13:30	**Erfaringer med Isolation Design Flow i Zynq-7000 FPGA fra Xilinx** Lech Tomczak , KDA	**Is your probe destroying your signal and then lying about the result?** Thomas Göransson, 4Test Instruments (Agilent)
14:00	**Adding the power of FPGAs to high performance server applications** Magnus Peterson, Synective Labs	**Design and integration of accelerators on the SHMAC multiprocessor platform** Per Gunnar Kjeldsberg , NTNU
14:30	**Game over! - This was Fxi Technologies** Torstein Dybdahl, TD Research AS	**Altera OpenCL: Maximising productivity on next generation Altera SoC Architectures** Bo Vinge-Brandt , EBV (Altera)
15:00	**Coffee break**	
Session 9	**Track AB: Closing Keynotes** Session chair: Atle Tangedal, Tekna	
15:15	**Closing Keynote: Eskil Skoglund, Head of Development, DolphiTech** DolphiTech - Long Story Short	
15:50	**Closing Keynote: Christian Rokseth, CEO, Bartec Pixavi** Building an international success based on organic growth, technology, enthusiasm and hard work instead of venture capital.	
16:25	Closing words	
16:30	The end	

Keynotes:

- Opening keynote: Adam Taylor, Head of Engineering
  - High Performance Imaging Solution Division, e2v
  What will ET make of My FPGA choice
- Closing keynote D1: Pat Mead – FAE Manager, Altera Europe
  How convergence is re-writing the FPGA industries development landscape
- Opening keynote D2: Jim Lewis, VHDL Training Expert, SynthWorks
  The Whys and Whats of Advanced Verification
- Closing keynote D2: Eskil Skoglund, Head of Development, DolphiTech
  DolphiTech - Long Story Short
- Closing keynote D2: Christian Rokseth, CEO, Bartec Pixavi
  Building an international success based on organic growth, technology, enthusiasm and hard work instead of venture capital.

See more info on the keynotes in the appendix.

List of exhibitors (for Wedn. 11th and Thur. 12th):

- 4Test www.4test.no
- Arrow Norway (Altera) www.arrowne.com
- Avnet Memec (Microsemi/Actel) www.microsemi.com
- Avnet Silica (Xilinx) www.silica.no
- Bitvis www.bitvis.no
- EBV (Altera) www.ebv.com
- FirstEDA www.firsteda.com
  (Aldec, OneSpin, Sigasi, SynthWorks)
- Innofour (Mentor) www.innofour.com
- MathWorks www.mathworks.com
- Synective www.synective.se
- Synopsys www.synopsys.com

FPGA-forum Program-committee:

- Arild Kjerstad, Kongsberg
- Hans Jørgen Fosse, Mikrokrets
- Jan Anders Mathisen, Silica/Xilinx
- Jim Tørresen, Universitetet i Oslo
- Atle Tangedal, Tekna
- Espen Tallaksen, Bitvis

Pre dinner party event - and entertainment during the dinner party

Wednesday @ 18:45. Starting the Dinner party:

Ut på tur med Stein P. Aasheim – en reise i bilder og livserfaringer
(Travelling with Stein P. Aasheim – a journey through photos and life experience)

Stein P. Aasheim is the nestor among Norwegian adventurers. Through a lifetime, he has challenged the forces of nature in all parts of the world – and for all altitudes. He will at FPGA-forum give us some samples from his many trips and expeditions. Although the talk will be in Norwegian, there will be numerous pictures/videos included.

Stein P. Aasheim er nestoren blant norske eventyrere. Gjennom et helt liv har han utfordret naturkrefter i alle deler av verden – og alle høyder over havet.

Se mer info på siste side i programmet.

During the Dinner party Wednesday

Candiss (Student choir)

Titles and Abstracts for presentations at FPGA-forum 2015

(In company alphabetical order)

Company & Presenter	Title & Abstract
4Test Instruments (Agilent) Thomas Göransson	**Is your probe destroying you signal and then lying about the result?** Learn tips and tricks about probing and how probe performance can be verified
ABB Anne Elisabeth Vallestad	**Exact Probability of Undetected Error (Pude) for shortened linear error-detection block codes via brute-force calculation in FPGA logic** Communication protocols routinely make use of 'shortened linear error-detection – sometimes error-correction - block codes', that is, add CRC to relatively short data words before transmission. Particularly for safety applications, it is important to standardization bodies to recommend codes whose Probability of Undetected Error (Pude) can either be exactly plotted over a range of bit error rates (BER), or has a well estimated or exactly calculated upper bound. However, formulas for exact Pude exist for maximum-length codes only. Example: for a 32-bit CRC the maximum length code word is 2**32 = ~4.3 billion bits. Nobody would use that in practice. For shortened versions of the same codes, we are left with crude upper bound estimates of Pude; or brute-force computation of the code's weight distribution from which exact Pude plots can be calculated. A code word's weight is the number of 1's it contains. Its weight distribution is a table of how many code words have weight 0, how many have weight 1, 2, 3, etc. up to weight n = the length of the code word. Brute force calculation of weight distribution involves counting through all possible values of the data part of the code word, and for each value: compute CRC, count the 1's of the code word (data + CRC part), and increment the correct 'weight bin'. For a data part length of, say, 48 bits, calculation time already grows to several days. However, working on the dual version of the shortened code – where the length of data part and CRC part are opposite of the original code - makes it manageable. A 50-year old mathematical trick takes the weight distribution for the dual code, and any given BER value, and transforms it easily to a point on the exact Pude plot for the original code. In this talk we will show how we calculated the weight distribution in FPGA for dual codes, based on original codes with CRC length up to 32 bits and data lengths up to 992 bits. Computing an up to 992-bit long dual-code CRC, calculating weights, etc. lends itself to FPGA implementation. A fully parallel/pipelined architecture was chosen in order to keep the calculation time reasonably short. Pretty far from our usual mindset where area and power consumption plays a major role.
Aldec	See FirstEDA
Altera Pat Mead	***** Closing Keynote day 1: How convergence is re-writing the FPGA industries development landscape** The emergence of next generation silicon technologies are driving the convergence of high performance processors and programmable FPGA fabric resulting in unprecedented levels of capability and flexibility. Coupled with high-level tool flow methodologies such as OpenCL and system level design tools, the industry's development landscape is evolving with never seen before levels of productivity and the enablement of non-traditional hardware design resource.
Altera	See Arrow and EBV
Arrow (Altera) Nikolay Rognlien	**Stratix10 HyperFlex Architecture** The HyperFlex architecture of Stratix10 will enable system clock speeds up to 1 GHz. Join this session to learn about the architecture, and how to use it efficiently.

Arrow (Altera) Nikolay Rognlien	**Powering FPGAs efficiently and easy.** Modern FPGAs has become more complex in their power supply demands to facilitate high performance. Altera's Enpirion product range is designed to solve these challenges. Learn about the products and how to use the power estimator to get suggestions on suitable power tree structures and dimensioning.
Avnet Memec (MicroSemi) Peter Trott	**SecureBoot-FPGA Anti-Tamper Solution** It has already been demonstrated that with the advanced security features of SmartFusion2, the family can be used within processor systems as a "Root of Trust" to securely validate and load application code on to any target processor. This can also be extended into loading application code into inherently vulnerable SRAM-based FPGA architectures. This paper will describe how this can be implemented. It will also show how side channel countermeasures and anti-tamper techniques can be applied to the Large SRAM-based FPGA systems.
AvnetSilica (Xilinx) Jan Anders Mathisen	**Real examples of embedded design in Zynq** The combination of modern FPGA technology and industry standard processor architectures in the same device is no longer a novelty. Does the combination live up to the promise of delivering unique design flexibility compared to the use of traditional design elements? The question will be addressed by presenting a few examples where processors and FPGA logic combine to create the best of both worlds. Throughout the presentation examples of methods, tools, IP and debug/analysis will be highlited.
Bartec Pixavi Christian Rokseth	***** Closing Keynote day 2: Building an international success based on organic growth, technology enthusiasm and hard work instead of venture capital** BARTEC PIXAVI is the smallest team ever to design a Smartphone and bring it to market. All R&D was done in-house.
Bitvis Sverre Vigander	**Register Wizard: Single source register information** Embedded systems invariably have configuration and status registers available to software. These registers need to be described in many different ways. Duplicated (redundant) information, i.e. information stored in several places, can easily get inconsistent. Maybe you add a new register, but forget to document it. Or you change a register address and forget to update the software header file. Register implementation in HDL is itself error-prone. The code is often copied from one register to another, and this commonly introduces copy-paste bugs, like updating the write portion but not the read portion. These problems are addressed with Register Wizard. With this tool, we take a single-source description of the registers and generate the necessary project files. The input files are based on the JSON format - an open, human-readable standard. With this simple description, Register Wizard generates the VHDL code for the registers, software header files and documentation. This ensures that all register description is in sync with each other.
Bitvis Espen Tallaksen	**UVVM: Universal VHDL Verification Methodology ("UVM for VHDL")** Most FPGAs and modules have two or more interfaces that need to operate simultaneously, and lots of corner cases arise from the access to these interfaces at more or less random times. Even a simple module like a UART has lots of corner cases - due for instance to the possibility of CPU reads of the RX-register coming at random times with respect to data actually entering the RX register/FIFO/buffer from the RX interface. To verify that all these corner cases are OK requires simultaneous stimuli (and monitoring) of all interfaces and the ability to skew these accesses with respect to each other. In most TBs this is handled in a very unstructured manner. Bitvis is now implementing UVVM, and as a first step we handle the most important functionality and the critical infrastructure for this. UVVM thus provides a simple, structured and reusable approach to the above problem. UVVM also allows random stimuli in a controlled manner. Like Bitvis Utility Library anyone can implement such a system, but it requires experience, structure and focus on simplicity. This presentation explains the system and how this significantly improves verification efficiency and quality. It also explains how UVVM compares to UVM at this level.

DolphiTech Eskil Skoglund	***** CLOSING KEYNOTE Day 2: 'DolphiTech - Long Story Short'** Stories, experiences & challenges of DolphiTech's journey through entrepreneurship, funding, bankruptcy, research, prototyping, development, market, customers, etc. On our way to become a success story. What does it take? - DolphiTech's story!
e2v Adam Taylor	***** OPENING KEYNOTE: 'What will ET make of My FPGA choice'** 'The last 20 years have seen the explosion of FPGA technology used in many different end applications, including those within harsh environments. It therefore follows that system developers wish these devices to operate correctly and safely regardless of environment. When engineers design for a spaceflight mission, there are a number of environmental factors that may impact mission performance: radiation; temperature; and the dynamic environment. How much weighting each of these environmental factors has depends upon the end space application which are typically grouped into one of three categories Launcher, Science / Exploration or Telecommunication. Regardless of the end application the engineer must consider FPGA technology, Mitigation strategies at both the FPGA and System level along with lessons learned from previous missions. However, these techniques and mitigation strategies are not just limited to space applications but can also be applied to terrestrial applications.'
EBV (Altera) Bo Vinge-Brandt	**Altera OpenCL: Maximising productivity on next generation Altera SoC Architectures** OpenCL for FPGAs from Altera make it possible to achieved a significant reduction in development time compared to traditional FPGA development flows. Altera's OpenCL for FPGAs combines the OpenCL parallel programming language with the parallel performance capabilities of FPGAs to deliver significantly higher performance and lower power consumption compared to multi-core CPUs and CPU/GPU-based systems. With OpenCL it is significantly easier for designers to accelerate their designs with FPGAs which has increasing relevance as Altera launch their next generation Arria 10 and Stratix 10 SoC architectures with densities extending to millions of logic elements
FirstEDA (Aldec/OneSpin) David Clift	**When failure is not an option! Static Verification For FPGAs** Static verification has been used in the ASIC industry for well over a decade now. Driven by safety critical and the ever increasing design complexity, static techniques are now being deployed by Europe's leading system companies designing with FPGAs. In this presentation we will discuss the static techniques Lint, structural design analysis, CDC analysis, and the use of formal for equivalence testing of FPGAs. We will evaluate and discuss the associated costs to deploy, the benefits, and the potential returns for a given FPGA program.
InnoFour (Mentor Graphics) Rick Stroot	**Bridging the FPGA World and the PCB** Today¹s powerful and extremely high pin-count FPGA¹s provide engineers with significant opportunities for increased features and more functionality whilst reducing the cost of their products. But with this increased complexity comes significant challenges in integrating these devices onto the Printed Circuit Board, with the need to map hundreds of logical signals to the physical pin out of the device whilst maintaining the electrical integrity of the design. This session will show not only how to ease the FPGA-on-board integration process by bridging the two worlds of HDL and PCB design but also how to guarantee the most optimum FPGA I/O design and physical implementation on the PCB significantly reducing both time-to-market and manufacturing costs.
KDA Kristin Aksnes	**Felles simuleringsmiljø gjør FPGAutviklerens hverdag enklere** - Presentasjon av KPS i Asker sitt simuleringsmiljø, - Hvorfor en fellessimulerings metodikk, - Hva skal til for å få til et felles simuleringsmiljø

KDA Lech Tomczak	**Erfaringer med Isolation Design Flow i Zynq-7000 FPGA fra Xilinx** Kongsberg Defence & Aerospace har vært med i EDA SoC prosjektet (European Defence Agency System on Chip). Som en del av prosjektet skulle vi lage en demonstrator basert på MicroZed evalueringskort for å prøve ut Single Chip Crypto konseptet. Kortet benytter ZYNQ FPGA XC7Z010 krets med et prosessorsystem med to ARM9 prosessorkjerner og en programmeringsdel. Prosjektet tok for seg implementasjon av to AES kryptomotorer og en komparator samt en random number generator. Alle moduler skulle isoleres og dette skillet skulle verifiseres. Vi har benyttet Isolation Design Flow (IDF) metoder med både ISE/Planahead og Vivado. Vi vil presentere våre erfaringer med dette prosjektet og legge spesielt vekt på IDF metodikk.
Mathworks Jonas Rutström	**FPGA and SoC Design from Idea to Implementation** Adopt, adapt, improve - High level design of FPGA and SoC solutions are rapidly gaining acceptance. Why? Because it is the future. We will inspire you to investigate new powerful solutions from MathWorks that will make your FPGA/SoC design super-duper. • Design higher and increase your flexibility • Use simulation to gain confidence in your design • Maximize your productivity with automated verification and implementation of FPGA and SoC designs • Partitioning of HW/SW systems using MATLAB/Simulink • From idea to product – different phases different tools!
Mentor Graphics	See Innofour
MicroSemi	See Avnet Memec
NTNU Per Gunnar Kjeldsberg	**Design and integration of accelerators on the SHMAC multiprocessor platform** In heterogeneous multiprocessor systems, a key aspect is the possibility of including specialized accelerators in individual processors. At NTNU a Single-ISA Heterogeneous Many-core Computer (SHMAC) is being developed in the strategic research group on Energy Efficient Computing Systems, both for use in master thesis projects and in research projects. This multiprocessor platform is implemented on a Versatile Express card with a Xilinx Virtex 7 FPGA. The presentation will give a short introduction to the SHMAC platform followed by examples of results related to integration of different accelerators on the platform.
Progbit Arin Morten Kjempenes	**Automatic register generation with corresponding protocol and APIs for simulation, lab test and final product access** There is a need for synchronizing the register information between fpga, sw, test sw (e.g. Tcl/LabView) and the documentation. A simple text format is developed for defining the registers and programs are developed for automatic generation of vhdl, c and Tcl code. The text file can be hand made or extracted from e.g a Word design specification with a simple script. The latter makes the design specification the single source for register definitions. Defining the registers is just the first step. Register access is needed in simulation, during lab (regression) test and in the final product. A simple protocol for accessing the registers is developed. The protocol basically transfer address, data, read/write ++. APIs in Tcl and c for accessing the registers via the protocol is developed. This can be used in simulation or in HW. So far the protocol has been implemented on RS232, JTAG and Ethernet(ip/udp). The commands, regression tests and APIs developed by the user in the simulator can be reused as is in the lab. The possibility of accessing the fpga independent of a uC/uP makes the fpga development partly independent of hw and sw. One can start developing in the simulator, then move to an evaluation board and use the jtag interface, then move to the final product via a direct JTAG/RS2323/Ethernet connection and then finally via the uC/uP where sw has access to the same register information via a simple data structure. The generated vhdl code is independent of the fpga vendor.

Synective Labs Magnus Peterson	**Adding the power of FPGAs to high performance server applications** In a wide range of industrial, military and academic applications, FPGAs used as coprocessors or streaming processors can boost the overall performance with 10x or more. Such systems will excel over traditional platforms in terms of power consumption, data processing speed, system bandwidth and system reliability - all at once. With this technology becoming mainstream, it has never been easier to benefit from it! This presentation will be a walkthrough of a handful of system examples and give an overview of where the technology stands today.
Synective Labs Lars Asplund	**VUnit - A Unit Testing Framework for VHDL** The interest for iterative and incremental development (IID) has increased over the last decade and has driven the development of tools, for example unit testing frameworks, to support IID. These tools have not been available outside the software community which has prevented VHDL developers from using known good practices. This presentation will show how VUnit, an open-source initiative for VHDL, closes this gap, how it has added value to existing projects, and how new users can get started.
Synopsys Antti Innamaa	**Synopsys HAPS Developer eXpress – Accelerated Transactors based IP prototyping case study** FPGA-based prototypes deliver high-performance operation and real-world connectivity but unless they can be brought-up and deployed early in the ASIC development project these benefits are of little use. This presentation is an elaboration of current FPGA prototyping market trends, the Synopsys HAPS Developer eXpress (HAPS-DX) platform, together with an introduction to a new prototyping paradigm - Transactors based FPGA prototyping.
SynthWorks Jim Lewis	***** OPENING KEYNOTE Day 2: The Whys and Whats of Advanced Verification** Verification can never get done soon enough, and this is particularly true as designs increase in size and complexity. This presentation discusses the whys and whats of transactions, code coverage – and its limitations, functional coverage, and randomization. While many verification languages focus using constrained random for everything, the sane approach is to use a mix methods (constrained random, intelligent coverage random, directed, algorithmic, and file based) and focus on getting verification done quickly. A big part of this is making sure that we maximize reuse throughout the test process.
TD Research AS Torstein Dybdahl	**Game over! - This was Fxi Technologies** A brief story about a startup from start to game over.
UiB (Universitetet i Bergen) Attiq ur Rehman	**Going from Virtex-2 pro to SmartFusion2 – Learning by doing (Mistakes)** The Readout Electronics of the ALICE TPC detector at CERN is being updated these days, where amongst others the existing Readout Controller Card, the Readout Control Unit (RCU) is being upgraded. There are two reasons for this: (1) We need an improved data rate, and (2) we need improved radiation tolerance. The main FPGA on the existing RCU is a Xilinx Virtex2-pro vp7, and this is too small to implement radiation tolerance measures on. Being an SRAM based FPGA it also experiences single event upsets in the configuration memory. When the upgrade project was initiated, it was decided to use the Microsemi SmartFusion2. This is a device that from the documentation is providing us with all the features that we need. It has a Microcontroller Subsystem, it has SEU immune flash configuration elements, it offers the opportunity for high speed serial links, and it has radiation hardened memory interface etc. However, porting the design from the Xilinx platform to the Microsemi platform has proven to be quite more challenging than what we first expected. This talk discusses these challenges, and what we have learnt when solving them.

UiO (Universitetet i Oslo) Chengxin Zhao	**Qualifying FPGAs for use in a Radiation Environment** This talk focuses on how to qualify FPGAs by means of irradiation campaigns. First we define two key parameters, flux and dose, and discusses what effects these have on different types of FPGAs. We further look into how to test the different elements in the FPGAs, that is configuration cells, SRAM, logic cells, PLLs and so on. The background of this presentation is the development and design of the readout electronics for the ALICE TPC at CERN. The Readout Control Unit (RCU), which is a key component in the readout electronics, is currently being upgraded to the RCU2. The main FPGA for the RCU2 is the Microsemi SmartFusion2..
UiO Jim Tørresen	**Five Years Context Switching of FPGAs – Ready to Start Executing?** Taking advantage of partial run-time reconfiguration can be used to reduce system cost and power or to raise performance. We have at University of Oslo in the project COSRECOS (Context Switching Reconfigurable Hardware for Communication Systems) funded by the Research Council of Norway (2009-2014) now for five years studied various ways of making run-time reconfiguration more applicable including by developing architectures, methods and tools that can contribute to dynamically changing configurations at run-time. The project results have been published in 30 scientific papers at high-impact international conferences and journal, four master thesis and two doctoral theses. By addressing the problem widely, we have in various ways prototyped systems, and demonstrated concepts that can contribute in making partial run-time reconfiguration of FPGAs more relevant to use, including in industrial products. This talk will contain an overview of some of the research results in the project as well as lessons being learned.
Xilinx	See Avnet Silica

FPGA-forum 2015, Wednesday 18:45

Ut på tur med Stein P. Aasheim
– en reise i bilder og livserfaringer




Stein P. Aasheim er nestoren blant norske eventyrere. Gjennom et helt liv har han utfordret naturkrefter i alle deler av verden – og alle høyder over havet.

Stein P. deltok på den første norske bestigningen av Mt. Everest, han har padlet og gått på ski gjennom Sibir, ridd gjennom Mongolia, syklet gjennom Sahara, krysset Grønland med Nansens utrustning, seilt til Antarktis, padlet gjennom Tasmania, gått til fots gjennom Ny Guinea og besteget de høyeste fjell i de fleste verdensdeler.

Foredraget inkluderer også inntrykkene fra

- -Familielivet i en liten fangsthytte på Svalbard
- -Den myteomspunnete og tragiske Trango-ekspedisjonen i 1984
- -På ski til Sørpolen i Roald Amundsens rute

Mer enn eksotiske eventyr

Stein P. understreker at kåseriet er mer enn bare et knippe med eksotiske eventyr, uoppnåelig for alle som ikke er tiltrukket av ekstremsport. Stein P. har utfordret tilværelsens yttergrenser. Det har gitt grunnlag for noen tanker og refleksjoner rundt livet.

-Dessuten har jeg noe å si både til våghalsene og barnefamiliene. Jeg har kombinert begge arenaene i 20 år, sier Stein P. Aasheim.

Bonus hvis du er misfornøyd.

Gratis guiding opp nordveggen på Romsdalshorn dersom foredraget ikke gir grunnlag for ettertanke!