Program for FPGA-forum 2012

Det 7. FPGA-forum - det norske FPGA-miljøets møteplass

FPGA-forum og utstilling: tirsdag 14. og onsdag 15. februar 2012
Britannia Hotel (Trondheim)

FPGA-forum er den årlige møteplassen for FPGA-miljøet i Norge. Her samles FPGA-designere, prosjektledere, tekniske ledere, forskere, siste års studenter og de største leverandørene på ett sted for 2 dagers praktisk fokus på FPGA.

Det blir foredrag fra norske bedrifter om utviklingsmetodikk og praktisk erfaring, universitetene presenterer nye og spennende prosjekter, og leverandørene stiller med aktuelle tekniske innlegg med et minimum av markedsføring. På utstillingen vil du kunne vurdere teknologi og verktøy fra de ledende leverandørene i bransjen.

FPGA-forum byr i tillegg på en ypperlig anledning til å møtes og utveksle erfaring innenfor FPGA-miljøet i Norge - både i pausene og under det sosiale arrangementet på kvelden.

Program tirsdag 14. februar 2012 (NB: Se abstracts bakerst i programmet.)

09.00	Registrering og kaffe.	
Sesjon 1	**Track AB** Sesjonsleder: Espen Tallaksen, TBD	
09.25	**Åpning**	
09.30	**Keynote by Clive "Max" Maxfield** Everything that can be invented has been invented…	
10.30	**Leverandørpresentasjoner** (3 minutter pr utstiller i alfabetisk rekkefølge)	
11:10	**Kaffepause**	
Sesjon 2	**Track A** Sesjonsleder: Ove Brynestad, Cisco	**Track B** Sesjonsleder: Solfrid Sjaastad, HiB
11.30	**FPGA in Microwave Radio Link** Svein Haustveit, Ceragon Networks	**FPGA-based Prototyping in the 40nm Era** Antti Innamaa, Synopsys
12.00	**"Senior", sandkorn i maskineriet for raskere og bedre produkt utvikling!** Tore Fleten, Cisco	**Quantifying the effect a radiation environment has on an SRAM based FPGA by using Fault Injection** Johan Alme, HiB
12:30	**Methodology Coordination; - Is it really needed?** Espen Tallaksen, Bitvis Design	**Assertions – A Practical Introduction for HDL Designers** Ian Gibbins, FirstEDA / Aldec
13.00	**Lunsj og Utstilling**	
Sesjon 3	**Track A** Sesjonsleder: Håvard P. Alstad, DataRespons	**Track B** Sesjonsleder: Hans Jørgen Fosse, Mikrokrets
14:15	**Programvare møter maskinvare – 2.0** Jan Anders Mathisen, Silica (Xilinx)	**Tackling the Five FPGA Implementation Challenges** Rick Stroot, InnoFour (Mentor Graphics)
14:45		**FPGAs in Algorithmic Trading with MATLAB and Simulink** Jonas Rutström, Mathworks
15:15	**Nanoscale Impulse Radar Sensor - System Level Modeling in SystemC** Dag T. Wisland, Novelda	Ingen foredrag i denne tidsluken. Dessverre kansellert av foredragsholder.
15.45	**Kaffepause og Utstilling**	
Sesjon 4	**Track A** Sesjonsleder: Espen Tallaksen, Bitvis Design	**Track B** Sesjonsleder: Jim Tørresen, UiO
16.30	**FPGA design from scratch** Sven-Åke Andersson, Realtime Embedded AB	**Presentasjon av Masteroppgaver** *Presentasjon av nominerte Masteroppgaver* *(se side 4)* *(NB: Kåring og prisutdeling under middagen)*
17:00	**Utfordringer og muligheter i FPGA-teknologien - hvor bør vi bevege oss?** Lars Eirik Mobæk, Cisco	
17.30	**Slutt – faglige presentasjoner.**	
19.30	Mottagelse i Lobby Lounge utenfor Speilsalen, Britannia Hotel	
20.00	Middag i Speilsalen, Britannia Hotell. - Underholdning: Studentkoret Pirum	

Program onsdag 15. februar 2012 (NB: Se abstracts bakerst i programmet.)

Sesjon 5	**Track A** Sesjonsleder: Johan Alme, HiB	**Track B** Sesjonsleder: Arild Kjerstad, Kongsberg
09.00	**PCIe-basert høyrate satellittmottaker** Øyvind Undstad, Kongsberg Spacetec	**OpenCL and hardware accelerator development for FPGA** Nikolay Rognlien, Arrow (Altera)
09.30	**Antifuse to Mercury** Jostein Ekre, Kongsberg Defence & Aerospace	**New Tools and Techniques for Building Run-time Reconfigurable Systems** Alexander Wold, Dirk Koch and Jim Tørresen, UiO
10.00	**SD-FX One year later** Torstein Dybdahl, FXI Technologies	
10.30	**Kaffepause og Utstilling**	
Sesjon 6	**Track A.** Sesjonsleder: Per Gunnar Kjeldsberg, NTNU	**Track B** Sesjonsleder: Magnus Jahre, NTNU
11.15	**LTDI – Laser Target Designator and Imager** Stein Kjølstad, Vinghøg	**Advanced FPGA Verification – VHDL -2008 and Static Design Rule Checks** Ian Gibbins, FirstEDA / Aldec
11.45	**FPGA i praksis** Hans Jørgen Fosse, Mikrokrets	**SoC development flow** Nikolay Rognlien, Arrow (Altera)
12.15	**Use of low cost FPGAs in high speed Data acquisition applications** Terje N. Andersen, Hittite	**Massive serial-parallel read-out system for the Focal detector** Kjetil Ullaland, UiB
12.45	**Lunsj og Utstilling**	
Sesjon 7	**Track A** Sesjonsleder: Arild Kjerstad, Kongsberg	**Track B** Sesjonsleder: Atle Tangedal, Tekna
14.00	**Lean SW Development for FPGA** Tore Fleten, Cisco	**FPGA i Datamaskinundervisningen ved NTNU** Magnus Jahre, NTNU
14.30	**Developing an FPGA module with a strong focus on efficiency, quality and modifiability** Espen Tallaksen, Bitvis Design	
15.00	Kaffepause	
Sesjon 8	**Track AB** Sesjonsleder: Jim Tørresen, UiO	
15.15	**Tredve år av digital kretsteknikk** Yngvar Lundh	
15.50	**FPGA, to SoC and beyond...!** Stefano Zammattio, Altera	
16.25	Avslutning	
16.30	Slutt	

Utstillerliste:

- 4Test www.4test.no
- Arrow Norway (Altera) www.arrowne.com
- Avnet Memec (Microsemi/ prev. Actel) www.avnet-memec.no
- Avnet Silica (Xilinx) www.silica.no
- Data Respons www.datarespons.no
- EBV (Altera) www.ebv.com
- FirstEDA (Aldec) www.firsteda.com
- Innofour (Mentor) www.innofour.com
- MathWorks www.mathworks.com
- Nortelco www.nortelco.no
- Synopsys www.synopsys.com

Rekrutteringshjørnet og Studentprosjekt:

- ARM www.arm.com
- GE Healthcare www.vividecho.com
- NTNU, Studentprosjekt
- Vinghøg www.vinghog.no

Prisutdeling (under middagen):

FPGA-Forums pris gis til beste masteroppgave innen FPGA.

Vurderingskomiteen består i år av Knut Wold, Høyskolen i Gjøvik, Hans Jørgen Fosse, Mikrokrets AS og Jim Tørresen, Universitetet i Oslo.

De nominerte er:

- Erik Strømme, NTNU
  ”Tone mapping in video conference systems”
- Arild Velure, Universitetet i Bergen
  “Design, implementation and testing of SRAM based neutron detectors”

Underholdning (under middagen):

Pirum (Fra Studentersamfundet i Trondheim)

Program-komitèen for FPGA-forum:

- Arild Kjerstad, Kongsberg
- Hans Jørgen Fosse, Mikrokrets
- Jan Anders Mathisen, Silica/Xilinx
- Jim Tørresen, Universitetet i Oslo
- Atle Tangedal, Tekna
- Espen Tallaksen, Bitvis Design

Abstracts for presentasjoner ved FPGA-forum 2012

(Alfabetisk rekkefølge på firmanavn)

Firma, Navn	Tittel, Abstract
Aldec	See FirstEDA
Altera Stefano Zammattio	**FPGA, to SoC and beyond...!** Ever since they first appeared on the market in the 80's FPGA devices have been an exciting technology with huge potential; over the last 30 years there have been many developments, both technical and commercial, that have driven FPGA technology and features to where they are today. In this presentation we will briefly review these developments and discuss the latest advances in FPGA technology, including the incorporation of hard ARM processor cores on to the devices. We will look at new technologies and consider the options that are available for future generations of FPGA device families. Despite the fact that FPGA's have been around for around 30 years the potential and opportunity for these devices has never been greater.
Altera	See Arrow
Arrow (Altera) Nikolay Rognlien Arrow Norway	**OpenCL and hardware accelerator development for FPGA** As the cost of FPGA devices continues to decrease whilst their DSP processing power increases, high performance computing developers are seeing FPGAs as a powerful and cost-effective platform for implementing hardware accelerators. With FPGA, finding a hardware platform with enough computing performance is generally not a problem, instead the main challenge is having a fast and effective design flow for developing algorithm implementations that run on the FPGA hardware. In this presentation we will describe an OpenCL based design flow for Altera FPGAs that will offer significant benefits to developers looking for ways to rapidly develop hardware modules for application acceleration.
Arrow (Altera) Nikolay Rognlien Arrow Norway	**SoC development flow** Description: Devices with the dual core ARM processors and FPGA on the same die are on the horizon, the flexibility and computing power of these devices will open a new set of applications that previously did not use FPGA. With the integration of FPGA and processor on one die come the challenge of how to develop applications on these devices. In this presentation we will explain how the Altera SoC FPGA device development flow works and how software developers will be able to cope with a changing processor specification.
Bitvis Design Espen Tallaksen	**Methodology Coordination; - Is it really needed?** Most companies have a strong focus on coordinating company critical processes, like sales, marketing, accountancy, department management, QA, etc. Lots of companies have also understood that project management is equally critical, but why is the development methodology treated so differently? Why do so many companies focus so little on coordinating their development methodology, - and what is the consequence of that?

Bitvis Design Espen Tallaksen	**Developing an FPGA module with a strong focus on efficiency, quality and modifiability** Many designers and project managers consider efficiency on one hand and quality and modifiability on the other hand to be inverse proportional. In other words improving the quality/modifiability has an efficiency penalty, and improving the efficiency results in lowering the quality. In most cases unfortunately - they are right. However, by properly structuring your module development you can in fact increase your efficiency while at the same time improving the quality and modifiability. It's all a question of methodology, implementation coordination and approach. This presentation will give a brief overview of some of the most important issues to consider - and show an example on how this could be applied to a real module design.
Ceragon Networks (former Nera Networks) Svein Haustveit	**FPGA in Microwave Radio Link** - Why Microwave Radio Link - Basic Architecture - FPGA Use and methods
Cisco Lars Eirik Mobæk	**Utfordringer og muligheter i FPGA-teknologien - hvor bør vi bevege oss?** FPGA-teknologien gir oss store muligheter med sin ytelse og fleksibilitet. Samtidig byr den også på problemer som høy kost, lite plass og treg utviklingshastighet. Denne presentasjonen tar for seg noen aktuelle problemstillinger for dagens FPGA'er slik som harde prosessorer, rekonfigurerbarhet og utviklingshastighet og kommer med noen forslag til hvordan vi kan utnytte teknologien bedre enn vi gjør i dag.
Cisco Tore Fleten	**"Senior", sandkorn i maskineriet for raskere og bedre produkt utvikling!** - Har "senioren" utspilt sin rolle i "moderne" produkt utvikling? - Sammenligner seniorens arbeidsoppgaver ved "gammel" og "moderne" produkt utvikling.
Cisco Tore Fleten	**Lean SW Development for FPGA** - Gjennomgang av prinsippene for "Lean SW Development". - Hvordan kan disse prinsippene brukes til FPGA utvikling? - Passer "Lean SW Development" for alle? - Vil "Lean SW Development" gå ut over kvaliteten på produktet?
FirstEDA / Aldec Ian Gibbins	**Advanced FPGA Verification – VHDL -2008 and Static Design Rule Checks** VHDL is still the most important hardware description language for FPGAs and ASICs in Europe. ALDEC will continue to support new VHDL standards with a high priority and is currently the leading supplier of VHDL 2008 simulators. VHDL 2008 offers some language enhancements for a more powerful and easier to use VHDL. Simulation is good for checking the functionality of the design against the expectations of the developer. Since VHDL is still intended to be a modeling language some constructs could cause functional differences between the RTL model and the synthesized gate level implementation. Static design rule checks are helping to recognize those issues in advance.
FirstEDA / Aldec Ian Gibbins	**Assertions – A Practical Introduction for HDL Designers** The majority of FPGA designers who are proficient in traditional HDLs might have heard about assertions, but haven't had time to try them out. Designers should be aware that assertions are quickly becoming standard part of both design and verification process, so learning how to use them is a future necessity. This presentation provides a quick and easy introduction to the basic ideas and applications of assertions: sequences, properties, assert and cover commands, etc. Along with practical examples.

FXI Technologies Torstein Dybdahl	**SD-FX One year later** SD-FX er en full verdig datamaskin inne i et microSD kort. For et teknologioppstarts firma så er det ingen rett vei frem til markedet eller ferdig produkt. Jeg vil fortelle hvordan det går og fremtiden for SD-FX. Historien om hvordan er nytt produkt blir til.
HiB Johan Alme	**Quantifying the effect a radiation environment has on an SRAM based FPGA by using Fault Injection** Single Event Effects is a major concern for electronic systems located in radiation environments. One such system is the Time Proejection Chamber (TPC) Readout Control Unit (RCU) of the ALICE experiment at CERN. The RCU is designed using an SRAM based FPGA that collects data from up to 3200 separate readout channels upon reception of a trigger. The RCU formats and ships these data to the DAQ system for storage and analysis. A Single Event Upset, which is defined as a radiation related bit-flip in a memory cell, may lead to corrupted data or, even worse, a system malfunction in the RCU. The latter situation will affect the operation of the ALICE detector since it causes a premature end of data taking. Because of the effect it has on the operation of the ALICE detector, it is of vital importance to estimate how often functional failures will occur with varying luminosity. One way of doing this is by using Fault Injection. This is essentially inserting bit flips in the configuration memory of the FPGA in a laboratory environment. Fault injection also provides an opportunity to investigate the cause of functional failures already seen during operation. In a heterogeneous and highly complex design such as the ALICE detector, it can be difficult to spot the origin of the error since there are so many physical devices and logical layers. Fault injection is thus an excellent functional test method that can be used in a controlled environment to decide whether the error is radiation related or not. This will help to improve the FPGA design and make it less susceptible towards SEUs.
Hittite Terje N. Andersen	**Use of low cost FPGAs in high speed Data acquisition applications** An affordable, USB powered 1GSPS Oscilloscope has been an industry target. To achieve this goal, both the ADC and the FPGA must have the combination of low cost, low power consumption and high speed. A complete Microwave-to-Bits Radio Receiver is another industry target as there has been no single vendor capable of providing the complete signal path from antenna to digital bits. This presentation shows how the Hittite ADC family utilizes Low Cost FPGAs to achieve both these goals. By utilizing the Hittite ADC and Xilinx FPGA Mezzanine Card (FMC) evaluation and prototyping platform, Hittite customers are able to • Achieve 1GSPS Oscilloscope operation with a USB power supply only. • Evaluate a complete RF/Microwave input signal to digital code receiver including digital filters and image rejection.
InnoFour (Mentor Graphics) Rick Stroot	**Tackling the Five FPGA Implementation Challenges** With design complexity being the #1 concern among FPGA designers, traditional implementation tools and methodologies are proving to be inadequate. System Houses need advanced, integrated solutions that unify the design creation and implementation process, deliver quality-of-results, reduce power consumption, allow for integration of 3rd party IP, and address industry-specific challenges such as lower power and mil-aero. This presentation will discuss five key challenges when implementing an RTL design to a final FPGA target. During this presentation you will learn: • How to unify design, verification, implementation, and PCB • Technologies to meet performance & area goals • How to reduce dynamic power consumption • How to adopt a device-neutral IP integration strategy • How to meet special requirements for mil-aero & safety-critical

Kongsberg Defence & Aerospace, div. Space Jostein Ekre	**Antifuse to Mercury** BepiColombo is an Interdisciplinary Cornerstone Mission to the planet Mercury, in collaboration between ESA and ISAS/JAXA of Japan. It consists of two scientific orbiters, the Mercury Planetary Orbiter (MPO) and the Mercury Magnetospheric Orbiter (MMO), which are dedicated to the detailed study of the planet and of its magnetosphere. The mission will commence in 2014 with the launch of the Mercury Composite Spacecraft (MCS) on Ariane V. The key challenges of the mission are to provide a safe transfer of the spacecraft carrying the scientific instruments to Mercury and to ensure successful science operations of both orbiters under extreme environmental conditions. Kongsberg Defense & Aerospace is developing the Solar Array Deployment Mechanisms and control Electronics (SADA). The SADA unit including electronics, mechanism and actuators is the main controller and driver of the Solar array of the Mercury Transfer Module (MTM). SADA will control MTM through a long interplanetary cruise. The Mercury Planetary Orbiter (MPO) and the Mercury Magnetospheric Orbiter (MMO) powered by the Mercury Transfer Module (MTM), will be delivered to their planetary orbits in 2020. The nominal mission will be completed by the end of 2021 with a possible extension of one more year. A brief on the units and the challenges will be presented.
Kongsberg Spacetec Øyvind Undstad	**PCIe-basert høyrate satellittmottaker** Kongsberg Spacetec har i mange satellittmottakssystemer basert på egenutviklede, FPGA-baserte kort med PCI-X interface. Tiden har lenge vært moden for å gå over til PCIe-interface. Prosjektet innebar ny teknologi, integrering av nye IP-er, oppgradering av gamle IP-er, en del nyutvikling og mye gjenbruk. Vi ser på hvilke utfordringer vi møtte underveis, og hvilke erfaringer vi sitter igjen med.
Mathworks Jonas Rutström	**FPGAs in Algorithmic Trading with MATLAB and Simulink** Today, approximately 70 % of the volume traded on the New York Stock Exchange (NYSE) is managed electronically. In 2007 commentators estimated that every millisecond reduction in response time would generate about $100 million a year. Today, the industry seeks single microsecond latencies. Such demands and the increasing need of processing parallel streams of financial information has led the financial industry to investigate the benefits of using FPGAs. In this presentation we will discuss the use of FPGAs in High Frequency Trading (HFT) within the financial industry and how MATLAB and Simulink can be used to develop trading algorithms and implement them directly onto FPGAs through HDL code generation.
Maxfield High-Tech Consulting Clive Maxfield	**Keynote: Clive “Max” Maxfield, Maxfield High-Tech Consulting** **Everything that can be invented has been invented…** …or so thought Charles H. Duell, who was the Commissioner at the U.S. Office of Patents in 1899. Fortunately for us, no one listened to Mr. Duell, otherwise we wouldn’t have gone on to create things like vacuum tubes, transistors, and silicon chips; and spaceships, smartphones, and tablet computers. The strange thing is that people continue to have a tendency to think “this is as good as it gets.” When the first FPGAs arrived in the scene in the early 1980s, for example, many engineers said that these components would only ever be useful in the context of implementing slow, simple logic functions. However, today we have devices running at hundreds of megahertz containing the equivalent of 20 million ASIC gates. Does this mean that we have finally reached the point where we can say “this is as good as it gets”? In his presentation, Max will consider many aspects of technology, from 2000-year-old steam engines to 200-year-old mechanical control systems to the latest-and-greatest in today’s FPGA technologies and some thoughts on what we might expect in the years to come…
Mentor Graphics	See Innofour

Mikrokrets Hans Jørgen Fosse	**FPGA i praksis** FPGA-ens fleksibilitet og mangfold gjør den til en viktig komponent i dagens embedded-systemer. Presentasjonen vil vise til eksempler på hvordan FPGA-ens egenskaper kan utnyttes til å kjøre tunge men samtidig allsidige applikasjoner. Presentasjonen vil også ta for seg noen av de utfordringene man møter knyttet til det å utvikle FPGA-løsninger basert på de nyeste kretsene.
Norautron Solutions AS Morten Larsen	**Simplify testing of embedded systems with Python** 'command-response' og 'response-only' type testing med - Både partiell og eksakt matching av respons - Protokoll-agnostisk: tekstlig påtrykk&respons eller binær, eller blanding - Regresjonstesting&selvlæring (record&replay) - Testmønster-lagring (databaseoppslag, dataentry & metoder)
Novelda Dag T. Wisland	**Nanoscale Impulse Radar Sensor - System Level Modeling in SystemC** The presentation will give an introduction to the Novelda UWB CMOS impulse radar and the fundamental principles behind the technology. The talk will in particular focus on the challenges in providing realistic system-level models for efficient design and verification. Results from the EU Artemis project "SYSMODEL" will be presented as an example of how to solve this challenge through the use of heterogeneous System-C based models. In addition different product applications and case-studies will be presented.
NTNU Magnus Jahre	**FPGA i Datamaskinundervisningen ved NTNU** Datamaskingruppa (Computer Architecture and Design Group, CARD) ved Institutt for Datateknikk og Informasjonsvitenskap har ansvaret for å undervise datamaskiners konstruksjon og virkemåte ved NTNU. Dette ansvaret strekker seg fra store, grunnleggende datamaskinfag med mange studenter til spissede fag på masternivå. I fagene Datamaskinkonstruksjon og Datamaskinprosjektet er bruk av FPGA et sentralt verktøy til å trene sentrale ingeniørferdigheter som å mestre kompleksitet gjennom abstraksjon og struktur. Denne presentasjonen vil presentere FPGA-systemene CARD benytter i undervisningen og hvordan disse systemene understøtter læringsmålene i de aktuelle fagene.
Realtime Embedded AB Sven-Åke Andersson	**FPGA design from scratch** As we say in Sweden: "Man kan inte lära gamla hundar att sitta" (You can't teach old dogs new tricks). But can you make an FPGA designer out of an ASIC designer. This is the question I will try to answer in my presentation by giving real life examples from my own experience. Since 1990 I have been designing ASICs together with many of the large ASIC manufacturers i.e. LSI Logic, Texas Instruments and IBM. These projects were multi-million dollar projects with more than 50 design engineers involved and could take two years to finish. When the silicon came back we could never be sure it would work. About five years ago I was aware that, with their increasing NRE costs and with long turnaround times, ASIC/ASSP/SoC design were becoming high-risk projects. Meanwhile, FPGAs had increased in capacity and performance to the extent that many companies were moving to using only FPGAs. Thus, I decided that it was time that I should learn more about FPGAs. I took the learning by doing approach and bought an FPGA development board and started experimenting. To keep track of my progress and to remember what I had learnt so far I decide to maintain an on-going record in the form of an "FPGA from scratch" blog.

Silica (Xilinx) Jan Anders Mathisen	**Programvare møter maskinvare – 2.0** Komplekse digitale systemer kombinerer som oftest det beste fra programvare og maskinvare for å gi optimal ytelse, kostnad, effektforbruk og utviklingstid. Embedded prosessering (innvevde systemer) i FPGA er en metode for å tilby fleksibel partisjonering og tettere integrasjon mellom programvare og maskinvare. Dette er ikke noen nyhet - men potensialet i metodikken er fremdeles langt fra fullt utnyttet. Kan nye prosessorsentriske FPGA'er og videreutvikling av høynivå designhjelpemidler bidra til det endelige gjennombrudd for optimalt samspill mellom programvare og FPGA (Hardware/Software codesign) og samtidig gi bedre produkter og redusert utviklingstid?
Synopsys Antti Innamaa	**FPGA-based Prototyping in the 40nm Era** FPGA-based prototyping has a solid foothold in the very heart of the design process of leading edge SoC, ASIC, IP and ASSPs projects. Advances in current 40nm FPGA devices have further provided exciting possibilities for the prototyping engineer. Synopsys has been at the forefront of turning such possibilities into realities, and the recent introduction of the Virtex-6 based HAPS-60 and HAPS-600 platforms prove to be no exception. The high performance, scalability and versatility of the systems provide designers with unparalleled verification, software development and system validation capabilities. This presentation is an elaboration of the next generation design methodologies, implementation platforms and system management techniques which empower designers of the 40nm era.
UiB Kjetil Ullaland (and Shiming Yang)	**Massive serial-parallel read-out system for the Focal detector** University of Bergen and University of Utrecht are developing a sandwich structure tower with 24 tungsten and silicon layers for future Forward Calorimeter upgrade of the Alice experiment. The readout electronics which is developed for the beam tests consists of 96 pixel sensors each with 4 data links at 160 MHz, which gives a total data throughput of more than 60 Gbps. Two sets of readout electronics are needed for the whole tower. For each there are two Spartan6 FPGAs utilized for the interface with front-end sensors, supplying clock and control signals and reading back digital data; automatic phase detection and delay adjustment ensure the correct sampling of input data. Synchronization of all data channels is obtained by bit alignment and test pattern verification, which gives a flexible solution for the issue of clock jitter and different cable/trace lengths of input data channel. A Virtex6 development board is used to collect data from the two Spartan6 FPGAs. An embedded Microblaze processor and a 256 bit AXI4 bus are the core components of the back-end readout system. The aligned data are sent to the Virtex board as a bus of 96 bits@160Mhz for every Spartan6 where a DMA engine via 256 bit@200Mhz AXI4 stream bus are storing the data in the local mass memory (DDR3 RAM). Petalinux is used for operation and control of the readout system and is also responsible for the external data flow, which is utilizing gigabit Ethernet. The external readout can be relaxed to gigabit rates since the effective beam time is only 5 %. Beam test is under preparation and preliminary result and performance figures will be presented.

UiO Alexander Wold, Dirk Koch and Jim Tørresen	**New Tools and Techniques for Building Run-time Reconfigurable Systems** Taking advantage of partial run-time reconfiguration can be used to reduce system cost and power or to raise performance. However, this comes at the cost of additional implementation steps. Because of a lack of adequate tools, reconfigurable system design has been time consuming and error prone, and in addition, the results often haven't shown substantial gains due to inefficient module integration techniques. Within the project COSRECOS, we have developed a new generation of tools that assist and automate the design of reconfigurable systems. Work also includes increasing the reconfiguration speed by enhancing the Xilinx ICAP interface with custom logic. By enabling overclocking of the ICAP interface, reconfiguration speed of up to 2.2 GB/s on Virtex-5 FPGA devices has been achieved. This is 5.5 times faster then the default configuration speed (400 MB/s) of Virtex-5 FPGA devices. Moreover, advanced module integration techniques have been developed to substantially remove logic and timing overhead among previous approaches. The talk will show that complex systems with various reconfigurable modules can be easily implemented with our tool GoAhead that supports all present Xilinx FPGAs. This tool provides floorplanning capabilities and constraint generation. Compared with the Xilinx vendor tools, GoAhead provides novel features, including zero logic overhead integration, hierarchical reconfiguration and module relocation (even among different systems).
Vinghøg Stein Kjølstad	**LTDI – Laser Target Designator and Imager** The LTDI is a fully integrated designator imager and rangefinder. It comprises a target designation laser (operating at 1.064µm and the Pulse Repetition Frequency (PRF) codes defined by STANAG 3733), a Rangefinder Receiver, a Laser Spot Imaging System (LSIS) camera, and all associated optics and electronics, all housed within a single enclosure with mechanical and electronic interconnection features to permit integration with the FOI2000 System. The LSIS camera has the see-spot functionality and provides system visual confirmation of the designated target, that allows laser guided munitions to be accurately deployed, thus minimizing collateral damage and enhancing the probability of success. The electronics comprises an FPGA that handles all video coming in and going out of the LTDI, synchronizing camera exposure to the laser pulse. Image processing routines implemented in the FPGA are both spatial and temporal.
Yngvar Lundh	**Tredve år av digital kretsteknikk** Teknisk ytelse og økonomi i komponenter og sifferkretser – digital elektronikk – har på få tiår utviklet seg dramatisk. Neppe har resultater av noen annen menneskelig aktivitet, kanskje noensinne flyttet grenser så langt. Mange muligheter. Vi minnes noen eksempler frem til åttiårene, ikke minst fra Norge.
Xilinx	See Silica