FPGA forum 2011

Tekna

Det 6. FPGA-forum - det norske FPGA-miljøets møteplass

FPGA-forum og utstilling: onsdag 2. og torsdag 3. februar 2011
Britannia Hotel (Trondheim)

FPGA-forum er den årlige møteplassen for FPGA-miljøet i Norge. Her samles FPGA-designere, prosjektledere, tekniske ledere, forskere, siste års studenter og de største leverandørene på ett sted for 2 dagers praktisk fokus på FPGA.

Det blir foredrag fra norske bedrifter om utviklingsmetodikk og praktisk erfaring, universitetene presenterer nye og spennende prosjekter, og leverandørene stiller med aktuelle tekniske innlegg med et minimum av markedsføring. På utstillingen vil du kunne vurdere teknologi og verktøy fra de ledende leverandørene i bransjen.

FPGA-forum byr i tillegg på en ypperlig anledning til å møtes og utveksle erfaring innenfor FPGA-miljøet i Norge - både i pausene og under det sosiale arrangementet på kvelden.

FPGA-forum Praktiske opplysninger

FPGA-forum 2011s konferanseavgift er kr. 5.200 for Teknamedlemmer, kr. 4.500 for forelesere og ansatte ved universitet/høgskole, og kr 6.200 for andre. Avgiften inkluderer deltakelse, bankett, og lunsj.
FPGA-interesserte studenter kan delta gratis på konferansen, men lunsj og bankett er ikke inkludert. (NB: Studenter må også melde seg på)

Rekrutteringshjørnet kjøres videre som i forfjor, der bedrifter kan sette opp en liten "stand" for rekruttering. Det er ingen ekstra kostnad forbundet med dette, men tilbudet gjelder kun registrerte (betalende) deltagere. Beskjed må gis til Espen.Tallaksen@Datarespons.no innen 21. januar.

Påmelding innen 21. januar 2011.

Ved avbestilling eventuelt uteblivelse, må hele kursavgiften betales. Hvis ønskelig kan en annen deltaker møte i stedet.

Overnatting på konferansehotellet koster kr 1095,- pr enkeltrom inkl. MVA. Hver enkelt deltager må selv kontakte Britannia Hotel (Dronningens gate 5) på tlf. 73 80 08 00 for bestilling av rom.
Rom må bestilles ASAP med referanse til Teknas FPGA-forum for å få denne sterkt rabatterte prisen.

Påmelding og informasjon under www.FPGA-forum.no

Program onsdag 2. februar 2011 (NB: Se abstracts bakerst i programmet.)

09.00	Registrering og kaffe.	
Sesjon 1	**Track 0** (Keynote intro ved Dirk Koch, UiO)	
09.30	**Keynote by Prof. Dr.-Ing. Reiner Hartenstein, Kaiserslautern University of Technology, CS dept.** We Need to Reinvent Computing to Avoid its Future Unaffordable Electricity Consumption	
10.25	**Leverandørpresentasjoner** (4 min per utstiller i alfabetisk rekkefølge)	
11:10	**Kaffepause**	
Sesjon 2	**Track 1** Sesjonsleder: Per Gunnar Kjeldsberg, NTNU	**Track 2** Sesjonsleder: Kjetil Svarstad, NTNU
11.30	**Vil FGPA dø?** Jon Østvand, T-Vips	**FPGA Design @ 28-nm** Antti Innamaa, Synopsys
12.00	***Automatisert lab-test av FPGA ved hjelp av JSystem*** Edvard Fosdahl, *Ericsson*	**Partial reconfiguration** Nikolay Rognlien, Arrow (Altera)
12:30	***Developing USB Crypto Adapter - Debug and Test Techniques*** Adnan Visic , *HDD*	**Accelerate FPGA Prototyping with MATLAB and Simulink** *Jonas Rutström, Mathworks*
13.00	**Lunsj og Utstilling**	
Sesjon 3	**Track 1** Sesjonsleder: Ove Brynestad, Cisco	**Track 2** Sesjonsleder: Solfrid Sjåstad Hasund, HiB
14:15	**Erfaringer med teknologiuavhengige FPGA-implementasjoner** Atle Sægrov, Radionor	**The challenges in system design, description and verification of run time reconfigurable systems... and how we might solve them.** Kjetil Svarstad, NTNU
14:45	**25 år med FPGA-teknologi - hva har det gitt oss og hvor går vi videre** Jan Anders Mathisen, Silica /Xilinx)	**Effektiv produktutvikling med eller uten kvalitet?** Eli Skyberg, Creo Development
15:15		**Design of embedded demonstrators using Altera DE2-cards** Per Gunnar Kjeldsberg, NTNU
15.45	**Kaffepause og Utstilling**	
Sesjon 4	**Track 1** Sesjonsleder: Espen Tallaksen, Data Respons	**Track 2** Sesjonsleder: Hans Jørgen Fosse, Flextronics
16.30	**Board bring-up av komplekse embeddedsystemer** Håvard Pedersen Alstad, Data Respons	***FPGA-forums pris for beste Masteroppgave:*** *Presentasjon av nominerte Masteroppgaver* *(se side 4)* *(NB: Kåring og prisutdeling under middagen)*
17:00	**Fra idé til produkt med Spartan-3** Jan Eide, Polewall	
17.30	**Slutt – faglige presentasjoner.**	
19.30	Mottagelse i Lobby Lounge utenfor Speilsalen, Britannia Hotel	
20.00	Middag i Speilsalen, Britannia Hotell. - Underholdning: Studentkoret Candiss - Pianobaren? eller Hjørnet?	

Program torsdag 3. februar 2011 (NB: Se abstracts bakerst i programmet.)

Sesjon 5	**Track 1** Sesjonsleder: Ståle Fiskvik, Mikrokrets	**Track 2** Sesjonsleder: Hans Jørgen Fosse, Flextronics
09.00 **09.30**	**Advances in Partial Runtime Reconfiguration – A Progress Report from the COSRECOS Project** Dirk Koch, Universitetet i Oslo	**Sophisticated FPGA Verification** Rick Stroot, Mentor Graphics / InnoFour
10.00	**Real time system level debug with system console** Nikolay Rognlien, Arrow (Altera) (Flyttet til track 1)	~~**Use of low cost FPGAs in high speed Data Converter (ADC/DAC) applications,** Terje Andersen, ASD~~ (Utgår pga. oppkjøp: Hittite Microwave Corporation Acquires Arctic Silicon Devices (ASD), a High Performance Mixed-Signal IC Company
10.30	**Kaffepause og Utstilling**	
Sesjon 6	**Track 1.** Sesjonsleder: Arild Kjerstad, Ericsson	**Track 2** Sesjonsleder: Kjetil Svarstad, NTNU
11.15	**SD-FX. The microSD application processor** Torstein Dybdahl, FXI Technologies	**De-embed using real time oscilloscope.** Thomas Göranson, Agilent Technologies /4Test
11.45	**Ekstrakt register informasjon fra VHDL til C-kode** Tore Fleten, Cisco	**World's first integrated FPGA, Cortex-M3 and Programmable Analog in a single chip solution** Rouzbeh Hosseinalikhani, Actel, (Microsemi)
12.15	**Designing safe FPGA internal clock domain crossings** Espen Tallaksen, Data Respons	**From Rapid Prototyping to Deployment with an** Integrated Software and Hardware Platform Stein Arild Nordrum, National Instruments
12.45	**Lunsj og Utstilling**	
Sesjon 7	**Track 1** Sesjonsleder: Atle Haga, Data Respons	**Track 2** Sesjonsleder: Eli Skyberg, Creo Development
14.00	**Test Driven Hardware Development - eller hvordan gjøre digital design enda morsommere** Ove Brynestad, Cisco	**FPGAs in industrial applications** Jørgen Hansen, EBV
14.30	**Zoom Audio: FPGA teknologi brukt i et mikrofonarraysystem for retninsgsstyrt lydopptak** Stig Nyvold, SquareHead Technology	
15.00	Kaffepause	
Sesjon 8	**Track 0** Sesjonsleder: Atle Tangedal, Tekna	
15.15	**Towards 50 billion connections with the help of integration** Johan Lassing, Head of TPU Microwave Core, Ericsson.	
15.50	**Fra Tandberg til Cisco - kultur og innovasjon** Olve Maudal, "Kunnskapsminister", Cisco	
16.25	Avslutning	
16.30	Slutt	

Utstillerliste:

- 4 Test AS — www.4test.no
- Acal BFI Norway (Actel) — www.acal.no
- Arrow Norway (Altera) — www.arrowne.com
- Avnet Silica (Xilinx) — www.silica.no
- Data Respons Norge AS — www.datarespons.no
- EBV — www.ebv.com
- Innofour (Mentor) — www.innofour.com
- MathWorks — www.mathworks.se
- National Instruments — www.ni.com/norway
- Synopsys — www.synopsys.com

Prisutdeling (under middagen):

FPGA-Forums pris gis til beste masteroppgave innen FPGA.
Pris-komiteen består i år av Kjetil Ullaland, Universitetet i Bergen, Knut Wold, Høyskolen i Gjøvik og Hans Jørgen Fosse, Flextronics.

De nominerte er:

- Rune Bergh Nilssen, NTNU
  ”Utvikling av et FPGA-basert system for emulering av CMOS digitalkamera med programmerbart signal-støy-forhold.”
- Elling Diesen, Universitetet i Oslo
  “A Run-time Reconfigurable Video Processing System”
- Erik Skogstad Næs, NTNU
  "Defect Pixel Correction"

Underholdning (under middagen):

Candiss (Fra Studentersamfundet i Trondheim)

Program-komitèen for FPGA-forum:

- Arild Kjerstad, Ericsson
- Hans Jørgen Fosse, Flextronics
- Jan Anders Mathisen, Silica/Xilinx
- Jim Tørresen, Universitetet i Oslo
- Atle Tangedal, Tekna
- Espen Tallaksen, Data Respons

Abstracts for presentasjoner ved FPGA-forum 2011

(Alfabetisk rekkefølge på firmanavn)

Firma, Navn	Tittel, Abstract
Agilent Technologies /4Test Thomas Göranson	**De-embed using real time oscilloscope.** DDR It is common for designers to want to measure a signal at a location that cannot be physically measured using an oscilloscope. The configurable system modeling allows you to remove the deleterious effects of unwanted channel elements, simulate waveforms with channels models inserted, view waveforms in physically un-probable locations, compensate for loading of probes and other circuit elements, and do so simply and quickly on the real-time oscilloscope. This technique becomes more important the higher the bitrate. This presentation will explain how you can add or remove signal path losses on your measurement and verify result directly on an oscilloscope. You can also add components and se how they effects measurement in real time..
Actel Rouzbeh Hosseinalikhani (Microsemi)	**World's first integrated FPGA, Cortex-M3 and Programmable Analog in a single chip solution** SmartFusion intelligent mixed signal FPGAs are the only devices that integrate an FPGA, ARM® Cortex™-M3, and programmable analog, offering full customization, IP protection, and ease-of-use. Based on Microsemi's proprietary flash process, SmartFusion FPGAs are ideal for hardware and embedded designers who need a true system-on-chip (SoC) solution.
Arrow (Altera) Nikolay Rognlien Arrow Norway	**Partial reconfiguration** Partial reconfiguration has up until recently been more of an academic exercise rather than usable in real design. With StratixV, Altera has introduced a userfriendly and safe partial reconfiguration. Join this session and learn the concepts.
Arrow (Altera) Nikolay Rognlien Arrow Norway	**Real time system level debug with system console** Debugging and board bringups are becoming more and more complex. Altera's System Console can be a great tool to ease these tasks. Join to see how System Console can be used in board bringup phase and to debug high level functionality in a high performance video system.
Cisco Tore Fleten	**Ekstrakt register informasjon fra VHDL til C-kode** Hvordan TANDBERG/Cisco har standardisert VHDL koden for automatisk ekstrahere register informasjon til C-kode.
Cisco Ove Brynestad	**Test Driven Hardware Development - eller hvordan gjøre digital design enda morsommere** Wikipedia: "Test-driven development (TDD) is a software development process that relies on the repetition of a very short development cycle: first the developer writes a failing automated test case that defines a desired improvement or new function, then produces code to pass that test and finally refactors the new code to acceptable standards." TDD metodikk kan også anvendes ved FPGA/ASIC utvikling. Mange av fordlene som oppnås ved softwareutvikling er dirkete overførbare til HDL basert utvikling. Foredraget viser hvordan dette kan gjøres og hvilke fordeler som oppnås på et praktisk eksempel.

Cisco Olve Maudal	Avslutningsforedrag dag 2: Olve Maudal, Cisco (Tandberg) **Fra Tandberg til Cisco - kultur og innovasjon**
Creo Development Eli Skyberg	**Effektiv produktutvikling med eller uten kvalitet?** Myter og sannheter rundt IOS9001, og erfaringer fra Creo Development AS; en liten utviklingsbedrift for embedded produkter
Data Respons Håvard P. Alstad	**Board bring-up av komplekse embeddedsystemer** Board bring-up av komplekse systemer kan være både komplisert og tidkrevende. Ved å gjøre noen enkle grep ved design, samt benytte seg av de mange mulighetene som ligger i en FPGA for effektiv debugging er det mulig å spare mye tid og finne feil fort og effektivt.
Data Respons Espen Tallaksen	**Designing safe FPGA internal clock domain crossings** Clock domain crossings (CDC) is probably the worst source of serious FPGA-bugs that can make your final product fail in fatal and mysterious ways. This presentation shows why this is a problem and how to handle the most common CDC scenarios. If time allows some of the most common misconceptions are also mentioned. Most issues here also apply 100% to ASIC development. This presentation is an excerpt from our two-day course “FPGA development Best Practices” (Originally a Digitas course).
EBV Jørgen Hansen	**FPGAs in industrial applications** How Altera help achieving the optimal project flow for implementation of integrated functional safety. a. Altera safety data package used for speeding up the project, sving time and cost. b. Altera devices used for minimizing the risk for expensive re-certifications. How to achieve highest efficiency in energy applications, using FPGA’s and multilevel IGBT’s. a. Using multilevel IGBT increases reliability and efficiency compared to standard IGBT. FPGA’s is the perfect controller for the multilevel IGBT. b. Demo/Video of FalconEye III, a FPGA based Multilevel IGBT motor drive.
Ericsson Johan Lassing	Avslutningsforedrag dag 2: Johan Lassing (Head of TPU Microwave Core), Ericsson. **Towards 50 billion connections with the help of integration** The race to upgrade the mobile networks for the exploding volumes of data communication is well underway. Driven by the end-users' thirst for high data volume services, mobile operators are forced to increase their transport capabilities radically, while getting little in return from their customers. This faces the operators with a multitude of challenges and the vendors have set out to support in this. Tomorrow's networks will have to combine the strengths from both the mobile world and the IP world and therefore the landscape as seen by the vendors today is about to change. The world is going mobile and the number of things connected to the networks is likely to increase in unprecedented ways. The topologies of the networks will have to change to accommodate this shift and this will force new innovating ways of handling radio access and radio transport. At the heart of this shift lies integration of hardware to enable more complex, less power hungry, but still cheaper technology, all in a rapidly changing system environment with unclear specifications. This talk will elaborate on the challenges of these contradictory requirements asking for the cost and power of ASIC with the flexibility of FPGA.
Ericsson Edvard Fosdahl	**Automatisert lab-test av FPGA ved hjelp av JSystem** Manuell test av FPGA-er på lab kan være en veldig tidkrevende prosess. Det kan medføre at vanlig test ikke har god nok dekningsgrad og at regresjonstest ikke blir kjørt. Ved hjelp av JSystem kan en komplett regresjonstest kjøres automatisk etter hver FPGA Place & Route for å sikre kvaliteten før man slipper dette videre til software-testing. JSystem er et open source rammeverk for å sette sammen testsuiter og kjøre disse. JSystem baserer seg på JUnit og testcaser skrives i Java. Vi har utviklet klasser for å aksessere FPGA-er og andre komponenter i systemet basert på dette rammeverket. Det vil bli gitt en introduksjon til systemet og erfaring fra et pågående prosjekt.

FXI Technologies Torstein Dybdahl	**SD-FX. The microSD application processor** How can you fit a multicore computerssystem insida a MicroSD card is 15mm(L) x 11mm(W) 1mm(H)? How can you build this from scratch? We will show you!
HDD Adnan Visic	**Developing USB Crypto Adapter - Debug and Test Techniques** This presentation covers the tools and techniques used for development of the FPGA part of Crypto Adapter. Crypto Adapter offers cost efficient encryption of thumb drives, external drives, and other USB-connected storage media. It incorporates the [hiddn]™ Crypto Module, highly certified (FIPS 140-2 level 3, CC EAL 4+ etc.) encryption device. Crypto Adapter consists of several different components including protocol adapters, PHY ICs, encryption devices and management unit implemented in FPGA. Due to certain restrictions in certification requirements, some of debugging techniques had to be avoided in final phases of development process. This presentation covers the different debugging and testing techniques used in different parts of the project. It will also highlight the advantages of using the FPGA during the development process and post release evolution of target products.
Kaiserslautern University of Technology Reiner Hartenstein	Keynote: Prof. Dr.-Ing. Reiner Hartenstein, Kaiserslautern University of Technology, CS dept. **We Need to Reinvent Computing to Avoid its Future Unaffordable Electricity Consumption** Under rising oil price at declining production the growing total energy consumption of all areas of computing will become unaffordable, maybe within a decade or earlier. But also energy consumption in general, as well as climate protection are key issues. Already now the carbon footprint of only the internet is higher than that of the worldwide air traffic. For the growth of its electricity consumption until the year 2030 a factor of 30 has been estimated, „if current trends continue“. Growing core counts of multi-core architectures are racing ahead of programming paradigms and programmer productivity. Programming research has stalled. The evolutionary path is not addressing key issues. Extrapolations from current methods are simply inadequate. For instance, multi-thread programming still seems to be a black art. Most supercomputing applications had originally been written for a single processor and now more than 50% of the applications do not scale beyond eight processor cores, although the newest peta-scale machines employ up to 100,000 processor cores each. For a future exa-scale machine system, expected in about 8 years, overall power consumption estimations range between 200 MW (power budget of the greater Karlsruhe area) and 10 GW, twice the power budget of New York City with a population of 16 millions. So we also have a power wall. The migration of applications from instruction set processors over to reconfigurable computing by FPGAs promises speed-up factors and energy saving „factors“ of up to several orders of magnitude. So we have two different paradigms for rewriting software: from control-flow-driven software to data-stream-driven configware, and, from single-core sequential software to manycore or multi-core parallel software, affected by the von Neumann syndrome and Amdahl’s law. Our industrial supply chain landscape is hitting a wall in developing next generation systems. For better verification, validation and major productivity gains similar as known traditional RTL to GDSII design flow we need abstraction levels „above“ RTL supporting interoperability between different design processes having far-reaching implications on design methods. Programming language support for yet-to-be developed higher level concepts is missing and remains weak even for current “low-level” concepts dealing with concurrency. Not expanding into new markets EDA design tool innovation has stalled. EDA experts are tied to the traditional semiconductor industry not investing in „expensive“ tools and are still struggling with understanding higher abstraction levels. System level design should be based on a new design science to address our needs in a fundamental way. However, present directions are not clear. Since we have to rewrite software anyway, we should use a twin-paradigm methodology to implement heterogeneous systems. For a successful transition we have to reinvent computing.

Mathworks Jonas Rutström	**Accelerate FPGA Prototyping with MATLAB and Simulink** Are FPGAs or ASICs your everyday business? Are they keeping you awake at night? Every day engineers and managers are facing shortening design cycles together with the need for increasingly complex devices. Simulating and verifying the behavior of the whole system is crucial for detecting design flaws in an early stage but is often seen as a challenge. What if you could take this one step further? What if you could use your simulation environment also to replace error-prone, manual methods of coding VHDL or Verilog? Come and see how MathWorks provides you with solutions to: • convert floating-point models to fixed-point • analyze the impact of fixed-point conversion early • use automatic HDL code generation to decrease development time • decrease verification time through HDL co-simulation • speed up prototyping with an FPGA turnkey implementation flow
Mentor Graphics / InnoFour Rick Stroot	**Sophisticated FPGA Verification** Verification is an area which is very expansive with new and extended languages, new methodologies and new features. SystemVerilog, VHDL2008, SecureIP, OVM (Open Verification Methodology), Assertions, Functional Coverage etc. In this session we will have a look at some of these that fits well into an FPGA verification environment. In specific we will have a look at Assertions and Functional Coverage, and will also touch on SecureIP, VHDL2008 and SystemVerilog. As a round up we will take a quick look at tools and methodologies that can help you take even more advantages of these new features in FPGA
National Instruments Stein Arild Nordrum	**From Rapid Prototyping to Deployment with an Integrated Software and Hardware Platform** In this session, learn how to design, prototype and deploy embedded systems using off-the-shelf tools and rapid prototyping hardware. You will see how fast design iterations can decrease the time you spend on requirements gathering, integration testing, and redesign – all of this ultimately adding up faster development with higher quality code. You will also learn how to rapidly prototype an embedded system, using off-the-shelf FPGA based hardware and migrate to lower cost deployment hardware. Several advanced applications, in the field of machinery control and oil&gas will be highlighted in this session.
NTNU Kjetil Svarstad	**The challenges in system design, description and verification of run time reconfigurable systems... and how we might solve them.** Most tools and research in run time reconfiguration (RTR) target the RTL level and down. System level design issues, however, such as design description and verification, will be important for RTR to be accepted also outside of the research community. We will present some of the research on these issues and the reasoning behind it, both on the conventional HDL level, for higher abstraction levels such as SystemC and functional descriptions, and we will, time allowing, present our suggestion for a new fundamental unit of design for RTR which leverages the dynamic objectives of RTR with familiar design fundamentals.
NTNU Per Gunnar Kjeldsberg	**Design of embedded demonstrators using Altera DE2-cards** In the spring of 2010, three master students at Department of Electronics and Telecommunications, NTNU, developed embedded demonstrators as their Master Thesis work. They all used the Altera DE2-cards as their development platforms. The goal was to develop demonstrators for use during, e.g., school visits, which in a good way show the advantage of using embedded systems due to the mix of hardware and software and the optimization potentials. The students made demonstrators of video presentation and manipulation, audio manipulation, and everyday electronic scenarios. The talk will cover the design process and the final results of the students.

Polewall AS Jan Eide	**Fra idé til produkt med Spartan-3** Polewall AS utvikler en frittroms optisk transceiver for bredbåndstilknytning. Produktet er designet rundt en Spartan-3 krets. Selskapet ble etablert i 2007, og var i begynnelsen et en-manns selskap. Det er i utviklingsarbeidet gjenbrukt en rekke moduler funnet på web, blant annet for data I/O og PicoBlaze design. Vi vil se litt nærmere på hvordan man kan bruke informasjon på web til å designe et komplett produkt med svært begrensede ressurser.
Radionor Atle Sægrov	**Erfaringer med teknologiuavhengige FPGA-implementasjoner** Abstract: Produkt-sykluser er ofte så lange at man tvinges til å migrere til nye FPGA-teknologier gjennom produktets levetid. For å redusere produktvedlikeholdskostnader er det ønskelig å holde designet så frikoblet fra de ulike FPGA-teknologiene som mulig. En teknologiuavhengig FPGA-implementasjon innebærer også en langt enklere og mindre risikofull migrasjon fra FPGA til ASIC. Foredraget belyser erfaringer ved bruk av tilgjengelig IP for softcore-implementasjon av CPU, memory og periferenheter o.l. i kildekodeformat.
Silica (Xilinx) Jan Anders Mathisen	**25 år med FPGA-teknologi - hva har det gitt oss og hvor går vi videre** Foredraget vil ta for seg utviklingen av FPGA-teknologi gjennom 25 år, se på typiske anvendelser og med dette som bakgrunn presentere tanker om videre utvikling
SquareHead Technology Stig Nyvold	**Zoom Audio: FPGA teknologi brukt i et mikrofonarraysystem for retninsgsstyrt lydopptak** Squarehead Technology utvikler, produserer og selger mikrofonarraysystemer som tilbyr helt nye muligheter for lydopptak i konferansesaler, auditorier, sportsarenaer og i TV-produksjoner. Kjernekomponenten er en mikrofondisk med inntil 345 innebygde mikrofoner og et vidvinkelkamera. Man kan velge vilkårlige opptaksposisjoner i et oversiktsbilde på en skjerm og ”zoome” inn lyd på samme måte som man zoomer i bildet med et kamera. All lyd kan om ønskelig lagres slik at man også kan zoome i ettertid. FPGA teknologi er benyttet for å tilfredstille krav til fleksibel datainnsamling, konfigurerbar pre-prosessering og skalerbarhet.
Synopsys Antti Innamaa	**FPGA Design @ 28-nm** In the 25 year history of programmable logic, every year has seen significant movements in the business and in the technology. 2010 was certainly no exception. In addition to the typical FPGA design characteristics closely monitored by FPGA designers – cost, speed and capacity, a new implementation metric emerged: Power. Silicon vendors have been quick to react to developments within the industry and indeed the year saw a number of exiting new announcements revealing innovative devices and technologies. For the designer this evolution implies the dawn of yet another degree of complexity - not only are there a number of fresh challenges to resolve, but also a variety of new resolutions to choose from. FPGA implementation tools are at the very heart of allowing for designers to successfully harness such complexity. At Synopsys, we are well prepared for next generation challenges by rolling out technologies such as team design for capacity and performance, fast turnaround time and “design preservation” flows for design closure and activity analysis for power reduction. This presentation is an elaboration of our implementation tool offering with reference to the key developments within the reconfigurable industry.
T-Vips Jon Østvand	**Vil FGPA dø?** De neste årene er det flere utfordringer med FPGA'er. Vanskeligere produksjon av FPGA'er gjør at kostnadene øker for produsentene. Store komplekse FPGA'er har lang kompileringstid, noe som fører til lengre utviklingstid for FPGA-baserte design. Konkurrerende teknologier klarer å utføre flere av oppgavene som FPGA'er gode til. Dersom det fortsatt skal være hensiktsmessig å bruke FPGA'er i systemdesign i framtiden må det fokuseres på disse utfordringene.

UiO Dirk Koch	**Advances in Partial Runtime Reconfiguration – A Progress Report from the COSRECOS Project** Within the COSRECOS project (Context Switching Reconfigurable Hardware for Communication Systems), new methods, tools and application examples are developed in order to simplify the design of runtime reconfigurable Systems on FPGAs. The talk will firstly introduce how we want to automate the design of reconfigurable systems. In addition, the talk will look back on the results of the COSRECOS project that have been achieved throughout the last year. This includes a novel easy usable design flow that provides powerful features such as module relocation or multi-module instantiation. Despite these capabilities, we are able to integrate modules with minimal logic overhead while providing high throughput communication. Furthermore, first results in automated floorplanning for both static and partial reconfigurable systems will be presented. Moreover, for boosting the reconfiguration processes in a system at runtime, techniques allowing a configuration speed beyond 2GB/s have been developed. The capabilities of runtime reconfiguration will be demonstrated in a number sorting FPGA accelerator that outperforms any Cell processor or GPU implementation.