FPGA 2006 forum

Det 2. FPGA-forum - det norske FPGA-miljøets møteplass

FPGA-forum og utstilling: onsdag 25. og torsdag 26. oktober

Scandic Hotel Prinsen, Trondheim

FPGA-forum er den nye årlige møteplassen for FPGA-miljøet i Norge. Her samles utviklere, prosjektledere og de største leverandørene på ett sted for 2 dagers praktisk fokus på FPGA.

Det blir foredrag fra norske bedrifter om utviklingsmetodikk og praktisk erfaring, og leverandørene stiller med aktuelle tekniske innlegg med et minimum av markedsføring. På utstillingen vil du kunne vurdere teknologi og verktøy fra de ledende leverandørene i Norge.

FPGA-forum byr i tillegg på en ypperlig anledning til å møte og utveksle erfaring innenfor FPGA-miljøet i Norge - både i pausene og under det sosiale arrangementet på kvelden.

FPGA-forum Praktiske opplysninger!

FPGA-forum 2006 konferanseavgift er kr. 4.000,- + mva for Abelia Innovasjons medlemmer og deltagere fra Universitet/Høgskole, og kr 5500,- + mva for andre. Den inkluderer deltakelse, bankett, og lunsj.

Avgiften vil bli fakturert etter at arrangementet er avholdt.
Ved avbestilling etter påmeldingsfristen, eventuelt uteblivelse, må hele kursavgiften betales. Hvis ønskelig kan en annen deltaker møte i stedet.

Overnatting på konferansehotellet koster kr 1014,- pr enkeltrom inkl MVA. Det er reservert rom på hotellet. Vi kan ikke garantere rom dersom reservasjon foretas etter 25. september 2006. **Hver enkelt deltager må selv kontakte hotellet på 73 80 70 00 for reservasjon av rom. Oppgi referansen DAK 241006**

Påmelding og informasjon: www.abelia.no > kalender

Program onsdag 25. oktober 2006

NB: Se abstracts bakerst i programmet.

Kl. 09.00	Registrering og kaffe. Knut Aune (Abelia Innovasjon)	
Sesjon 1: Åpningssesjon. Sesjonsleder: Espen Tallaksen (Digitas)		
09.30	Atmel, Gaute Myklebust	Kan man drive avansert utvikling i Norge?
10.10	Aurotech, Audun Græsli	FPGA-teknologi bryter barrierer innen medisinsk ultralyd
10.35	Mentor, Lars Gustafson	Raising the level of FPGA design
11.00	Pause	
11.30	GE Healthcare, Morten Haugen	How to fit complex signal processing algorithms into reasonable sized FPGAs
11.55	Leverandørpresentasjoner.	Kort info fra alle utstillere
12.55	Lunsj og utstilling	

Sesjon 2. Sesjonsleder: Jim Tørresen (Universitetet i Oslo)		
14.20	4Test, Thomas Gøransson (Agilent)	FPGA analye og feilsøking.
14.45	Tandberg Storage, Einar Inge Ellingsen	FPGA-prototyping
15.10	Mikrokrets,	FPGA utviklingsmetodikk
15.35	Pause	
16.05	NTNU, Pauline Haddow	Towards Complex, Reliable, Adaptive, Bio-inspired FPGA systems
16.30	Synplicity, Ola Wall	Latest advances in EDA for FPGA users: a year is a long time in FPGA
16.55	Kitron, Geir Åge Noven	Generering av VHDL-kode for on-chip TDM-nettverk
17.20	PLDA, Kate Martin	PCIe as an On-board System Bus
17.45	Slutt – faglige presentasjoner.	

19.30	Mottagelse ved Speilsalen, Britannia Hotell
20.00	Middag i Speilsalen

Program torsdag 26. oktober 2005

NB: Se abstracts bakerst i programmet.

Sesjon 3. Sesjonsleder: Arild Kjerstad (Ericsson)		
09.00	Høgskolen i Bergen, Ketil Røed	Irradiation testing of FPGA-based readout-electronics for a large tracking detector
09.25	Høgskolen i Bergen, Johan Alme	Active Partial Reconfiguration of a Xilinx Virtex-II pro FPGA.
09.50	MathWorks, Jan Hedmann	Streamlining FPGA Implementations of Signal Processing Algorithms Using Model-Based Design
10.15	Pause	
10.45	Altera, Stefano Zammattio	FPGA the future of system development
11.10	Konsberg Defence Com., Roar Skogstrøm	Kommandostyrte testbenker i VHDL
11.35	Konsberg Defence Com., Simen G. Hansen	Avansert metodikk for divisjon og kvadratrot
12.00	Xilinx, Jan A. Mathisen	Embedded prosessering I FPGA - Veien videre
12.25	Lunsj og utstilling	

Sesjon 4. Sesjonsleder: Hans Jørgen Fosse (Mikrokrets)		
13.30	Actel, Rouzbeh Hosseinalikhani	Integrating an ARM Softcore into an FPGA
13.55	Nordic Semiconductor, Jon E. Oterhals	Hardware /firmware co-development using FPGA
14.20	Digitas, Espen Tallaksen	Simple Verification Components, for better and faster testbench development.
14.45	Pause	
15.15	Tandberg, Tore Fleten	HD-Kamera – fra ide til serieproduksjon på 1 år
15.40	Tandberg, Tore Fleten	Dokumenter VHDL med hjelp av shareware programmet VHDLDOC
16.05	Einar Aas	Moore's lov sett i lys av FPGA
16.45	Slutt	

Utstillerliste:

Firma:	Web-adresse:
4test	www.4test.no
Acal Norge (Actel)	www.acal.no
PLD Applications	www.plda.com
Nortelco Electronics	www.nortelco.no
Arrow Norway AS (Altera)	www.arrownordic.com
Synplicity	www.synplicity.com
Mentor Graphics	www.mentor.com
Xilinx	www.xilinx.com
The MathWorks	www.mathworks.com
Mikrokrets	www.mikrokrets.no

Prisutdeling (under middagen):

BLADET ELEKTRONIKK OG MIKROELEKTRONIKK-FORUMS
PRIS FOR BESTE HOVEDOPPGAVE
INNEN MIKROELEKTRONIKK-KONSTRUKSJON
VED INSTITUTT FOR ELEKTRONIKK og TELEKOMMUNIKASJON, NTNU

Abstracts, Onsdag	
09.30	Kan man drive avansert utvikling i Norge?
10.10	FPGA-teknologi bryter barrierer innen medisinsk ultralyd
10.35	Raising the level of FPGA design With newer FPGA's the complexity has skyrocketed. Not only in the number of gates and resources available inside of the FPGA's but also for the tools available for the designer to cope with. To start with the designer needs to have a functional model of his system so that he can do exhaustive analysis on the functionality. To do so one of the basic features he needs to implement into his model is bit-accurate datatypes. We will introduce the AC, or Algorithmic C - dataypes that solves this problem. Next step is probably that since most of the design doesn't start from scratch is to reuse old code, but is that really practical? We will show you a method for predicting the reuse-effort to help you get the RTL faster into your system. For new functional blocks that needs to be designed, why don't you raise the level of abstraction to C++? If you take the advantage of having a very fast C++ model for your system, we will also show you that it is possible to take that model and create very good HW out of it. One of the parts that is often overlooked in the FPGA process is the pinouts. With parts available in packages upto 1700+ pins this has become a very labourously task indeed and we will show an easier way to do this. In the process the manual steps traditionally taken is taken away and you get much better quality of the PCB layout first time! Lastly the RTL code has to be synthesized for the FPGA technology, and here the role of the synthesis tool has changed somewhat. From being just a synthesis tool, it now also needs to be very good at analysis to help you find all those hard-to find timing problems that can exist in multi-clock systems.
11.00	Pause
11.30	How to fit complex signal processing algorithms into reasonable sized FPGAs
11.55	Leverandørpresentasjoner
12.55	Lunsj og utstilling
14.20	FPGA analye og feilsøking. Agilent Technolonies har utviklet et verktøy (Dynamisk Probe) som gir deg enklere tilgang og er mere fleksibel når en feilsøker FPGA i sanntid. Den nye ATC2 vil hjelpe deg med tilgang til interne signaler i din FPGA, måle i sanntid og samtidig få innbyrdes målinger av andre "busser" i systemet.
14.45	FPGA-prototyping
15.10	FPGA utviklingsmetodikk
15.35	Pause

16.05	Towards Complex, Reliable, Adaptive, Bio-inspired FPGA systems This presentation will introduce a number of ongoing research projects of the CRAB lab at IDI, NTNU where FPGA technology plays an important role. In each project presentation, particular focus will be given to how the project challenges or exploits the current FPGA architecture. The projects range from non-conventional design techniques, through fault and defect tolerance, hardware modelling of biological processes to highly parallel processing.
16.30	Latest advances in EDA for FPGA users: a year is a long time in FPGA EDA for FPGA is a never-ending task and in fact, the task becomes ever-more demanding. The capacity and complexity of the latest FPGAs require a step up in design flow sophistication. The challenges are already promoting new tools solutions . . . • Synthesis and Place&Route will become merged in order to obtain timing closure and shorten iteration time. • Debug capability needs to be promoted in importance and become more than an afterthought "if the FPGA doesn't work on board". • The sheer size of the largest devices will require system-Level design tools in fill them in time to meet ever shorter design cycles. • A secure methodology must be found in order to promote a healthy third-party IP market for FPGA. • Synplicity has embraced these challenges with the creation of new tools for high-level synthesis, timing closure and on-board debug. This presentation will give details of some of these developments and will be of specific interest to FPGA designer who wishes to keep up to date with the rapid changes in FPGA design tools.
16.55	Generering av VHDL-kode for on-chip TDM-nettverk
17.20	PCIe as an On-board System Bus More than just a high-speed data link, the PCI Express protocol defines sub functions (end point, root port, switch, bridges) that can be used to build a dedicated networking system on a board and solve application specific architecture challenges. The presentation illustrates such a system with a case study of a real application.

Abstracts, Torsdag	
09.00	Irradiation testing of FPGA-based readout-electronics for a large tracking detector An SRAM-based and a FLASH-based FPGA have been irradiated with protons (29, 35 and 180 MeV) and neutrons (90 MeV) in order to qualify their radiation tolerance for a particle detector environment. Irradiation tests have been carried out at the Oslo Cyclotron (OCL), University of Oslo, and at The Svedberg Laboratory (TSL), Uppsala University. Irradiation test methodology and results will be presented along with an introduction to the related radiation effects.
09.25	Active Partial Reconfiguration of a Xilinx Virtex-II pro FPGA. Any SRAM based FPGA will experience errors in the configuration memory when irradiated with a sufficient large particle flux. These errors are called single event upsets. A single event upset may lead to a single event functional error, which is defined to be an error that has a measurable effect on the operation of the firmware. To reduce the chance of this to happen, Xilinx FPGAs has a feature that makes it possible to reload parts or the complete configuration memory without interrupting operation. This is called active partial reconfiguration. A solution for this has been developed for a data readout electronic system that is a part of a detector physics experiment to be commissioned at CERN in the near future.
09.50	Streamlining FPGA Implementations of Signal Processing Algorithms Using Model-Based Design Implementations of signal processing systems on FPGAs require a continuous design flow that includes system design, HDL design, and system simulation and verification. Ensuring that the FPGA implementation matches the system specification is a key part of the verification process. Yet, many system engineers and FPGA designers continue to employ a manual 'bit-true' verification methodology involving multiple tools, manual processes, and Perl scripts. This is often a laborious and error-prone activity involving file exchanges between the system designer and the FPGA designer. Geographically diverse teams face even bigger challenges in this regard since the system designer and the FPGA designers are not sitting in the same location. What is needed, then, is a design methodology that bridges the world of system designers, and the FPGA designers to increase productivity and produce 'correct-by-construction' designs that match the system specification. This presentation will illustrate how Model-Based Design provides the benefits of top-down and bottom-up design methodologies to help quickly achieve the design objectives. Using an 'executable design specification', the presentation will discuss how Model-Based Design streamlines FPGA implementations of signal processing algorithms.
10.15	Pause
10.45	FPGA the future of system development Traditionally, the heart of any system is the processor and the system is built around the performance, features and deficiencies of that processor. Over the last few years however systems have been moving to multi-processor architectures to address more demanding application performance and power efficiency requirements. In order to reduce costs, designers require processors that are tailored to fit their solution, in response to this processor vendors are responding by developing more versions of their processor devices. In today's embedded markets creating a successful product is increasingly dependent on factors like being first to market, rapid cost reduction and effective marketing rather than technical superiority. In this presentation we will show how FPGA devices and embedded tools can enable you to rapidly develop low cost, high performance embedded systems.

11.10	Kommandostyrte testbenker i VHDL KDA Communications bruker kommandostyrte testbenker i VHDL ved FPGA utvikling. Presentasjonen vil gjennomgå kommandospråket som benyttes, og hvordan VHDL testbenken leser inn og tolker kommandoene fra tekstfiler. Alle VHDL funksjonene som inngår er gjenbrukbare. Det vil gis eksempler og erfaringer fra praktisk bruk i utvikling av flere FPGA'er
11.35	Avansert metodikk for divisjon og kvadratrot Presentasjonen vil gjennomgå hvordan divisjon og kvadratrot kan implementeres effektivt i FPGA teknologi. Subraktive og multiplikative algoritmer for divisjon og kvadratrot vil bli gjennomgått og sammenlignet. Det vil bli gitt eksempler fra praktisk bruk av multiplikative algoritmer i FPGA og ASIC utviklet ved KDA Communications
12.00	Embedded prosessering I FPGA - Veien videre
12.25	Lunsj og utstilling
13.30	Title: Integrating an ARM Softcore into an FPGA. The ARM7 is the most widely used 32-bit processor ever, and now it's available as a soft IP in FPGAs, with the flexibility to configure the peripherals to better fit the system you are building. - ARM Processor background - ARM core configuration & setup - Implementing the Core into the FPGA - FPGA Development tools, and supported FPGA's - ARM Development tools
13.55	Hardware /firmware co-development using FPGA I presentasjonen så vil jeg vise hvordan vi benyttet FPGA i de forskjellige utviklingsstegene for nRF24Z1, som er en RF transiever med en innebygd 8051 med tilhørende firmware + et hardware audio interface. 1. Alle analoge blokker ble samlet i en modul i ASIC designet, som så ble byttet ut med en FPGA spesifikk implementasjon. Her vil jeg komme med en del tips og ideer for hvordan forskjellige analoge blokker kan modelleres. 2. Prototyp versjon av kretsen ble laget med en spesiell modus der en lett kunne benytte de analoge blokkene i ASIC men fremdeles beholde 8051 og annen digital-logikk på FPGA. 3. For å bedre debugmulighetene for 8051 plattformen ble de nødvendige pinner rutet ut for å interface en standard 8051 In Circuit Emulator. 4. For å bytte innhold i "Rom" på FPGA, ble data2mem scriptet benyttet sammen med Impact og videre integrert sammen med Keil compilatoren.

14.20	Simple Verification Components, for better and faster testbench development. - Brief introduction to efficient verification through structured testbenches and simulation - Building up a verification environment - A first step to simple verification components - and really efficient verification - Why verification reuse is so efficient - even within a single complex FPGA project The presented methodology is totally language and technology independent. It is a methodology that should be used by all designers, but has been embraced mainly by companies with strict requirements to time to market. This presentation has a major focus on how to get started with no overhead.
14.45	Pause
15.15	HD-Kamera – fra ide til serieproduksjon på 1 år • TANDBERG erfaring fra algoritme implementere i DSP'er til bruk av FPGA. • Softcore prosessor – førstegangs erfaringer. • Team arbeid mot felles FPGA
15.40	Dokumenter VHDL med hjelp av shareware programmet VHDLDOC
16.05	Moore's lov sett i lys av FPGA Vi ser på Moores lov slik den ble fremstilt i Electronics i April 1965. Senere kom de mer solid funderte veikartene for halvlederindustrien, nå kalt ITRS Roadmaps. Vi tar en liten sveip innom noen av disse veikartene, og forsøker å finne budskap særlig egnet for FPGA-utvikling. Dette blir en høyst uformell presentasjon.